

Fig. 1
(PRIOR ART)

Fig. 2

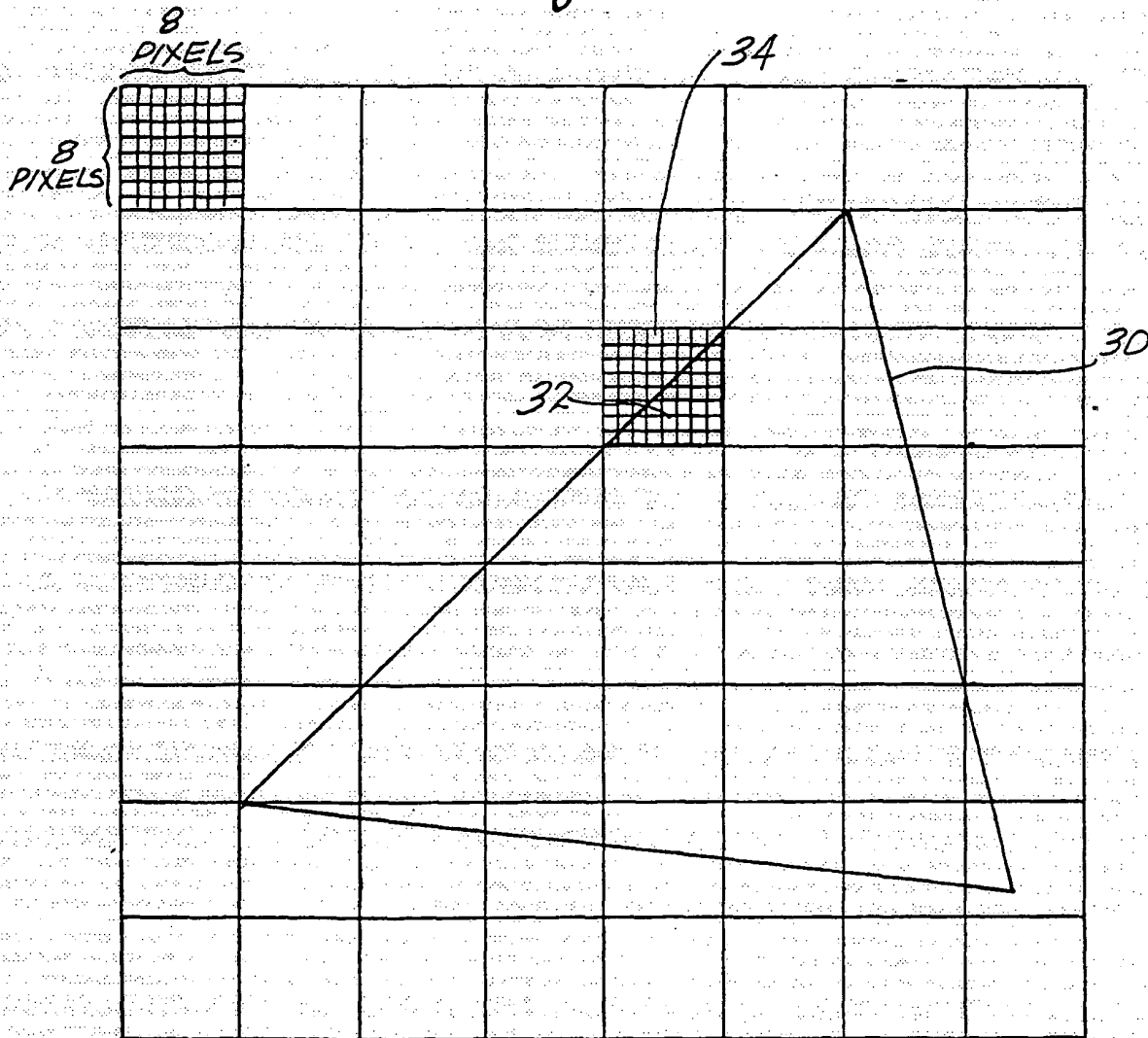


Fig. 3

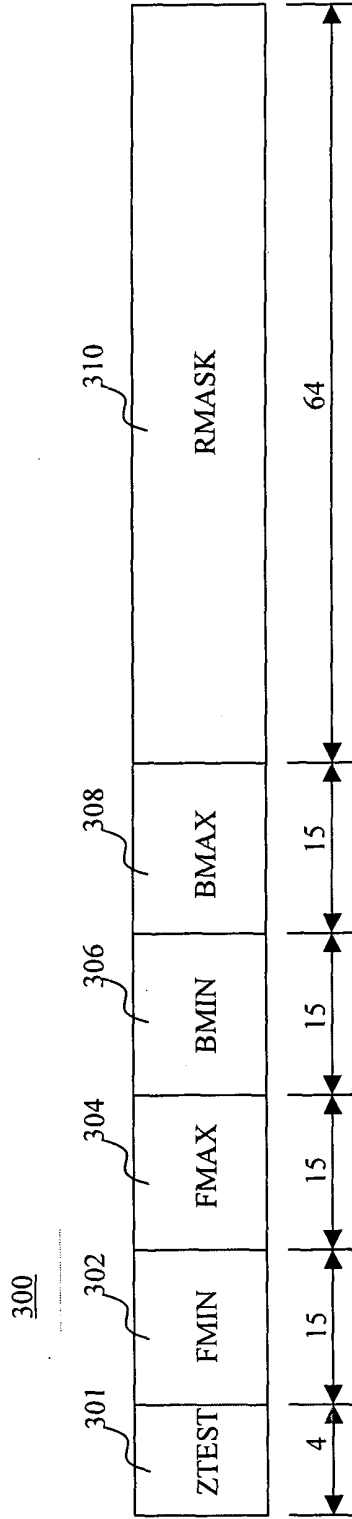


Fig. 4A

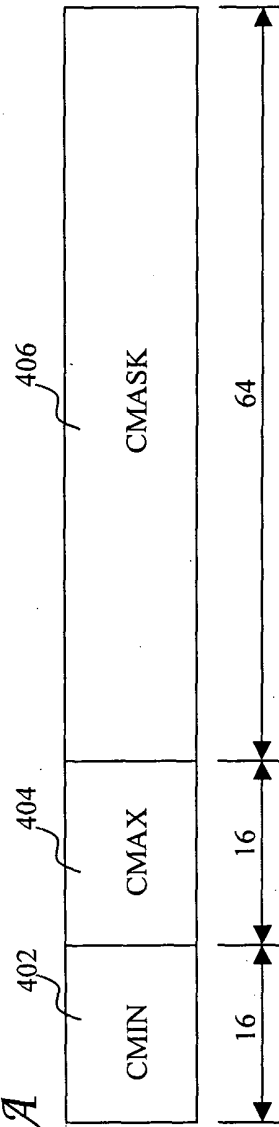


Fig. 4B

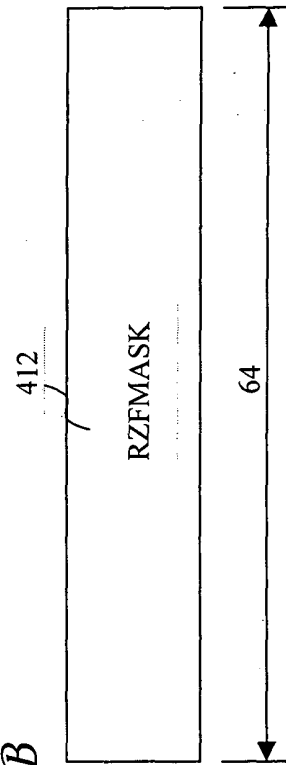


Fig. 5

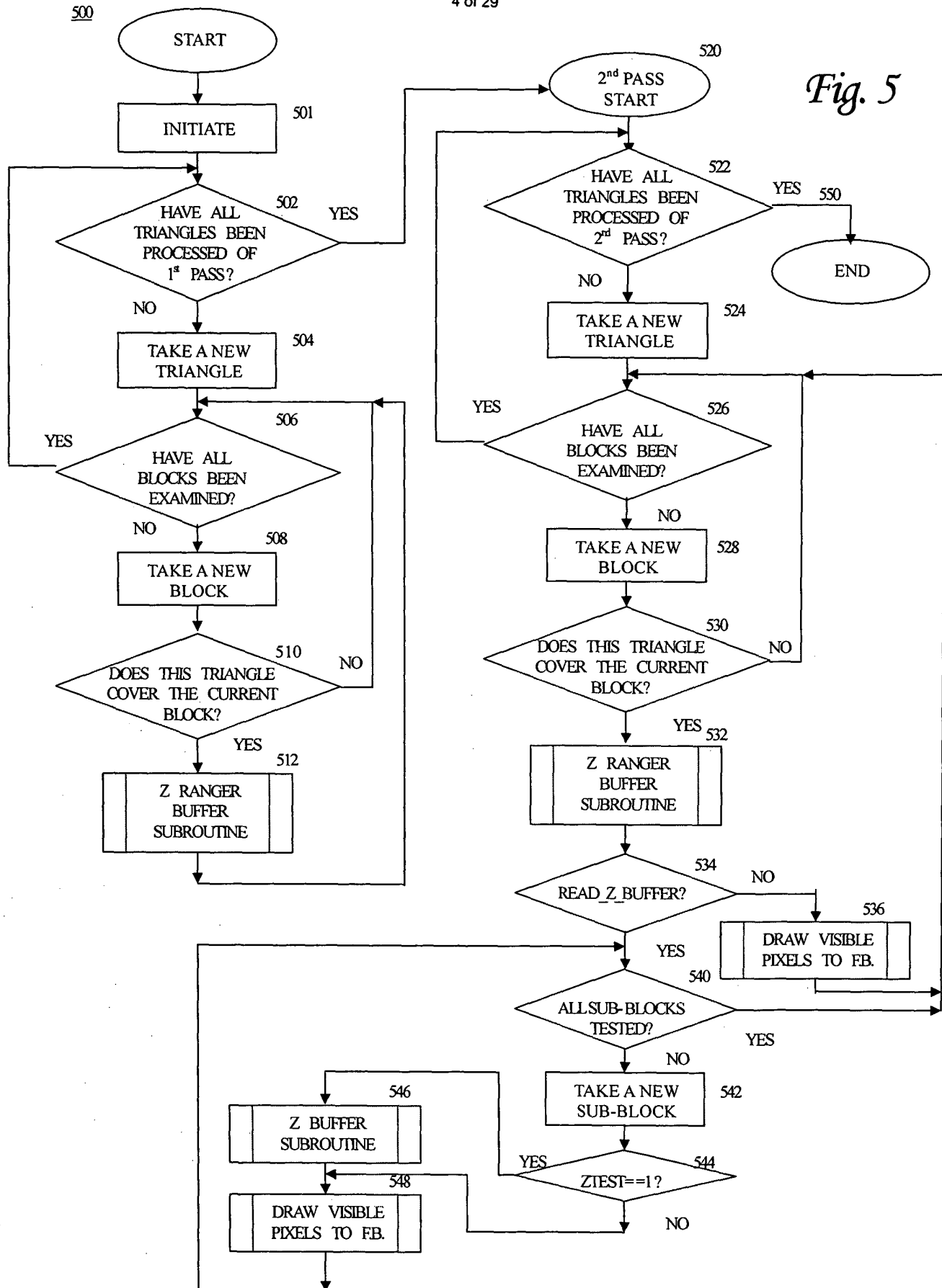


Fig. 6A

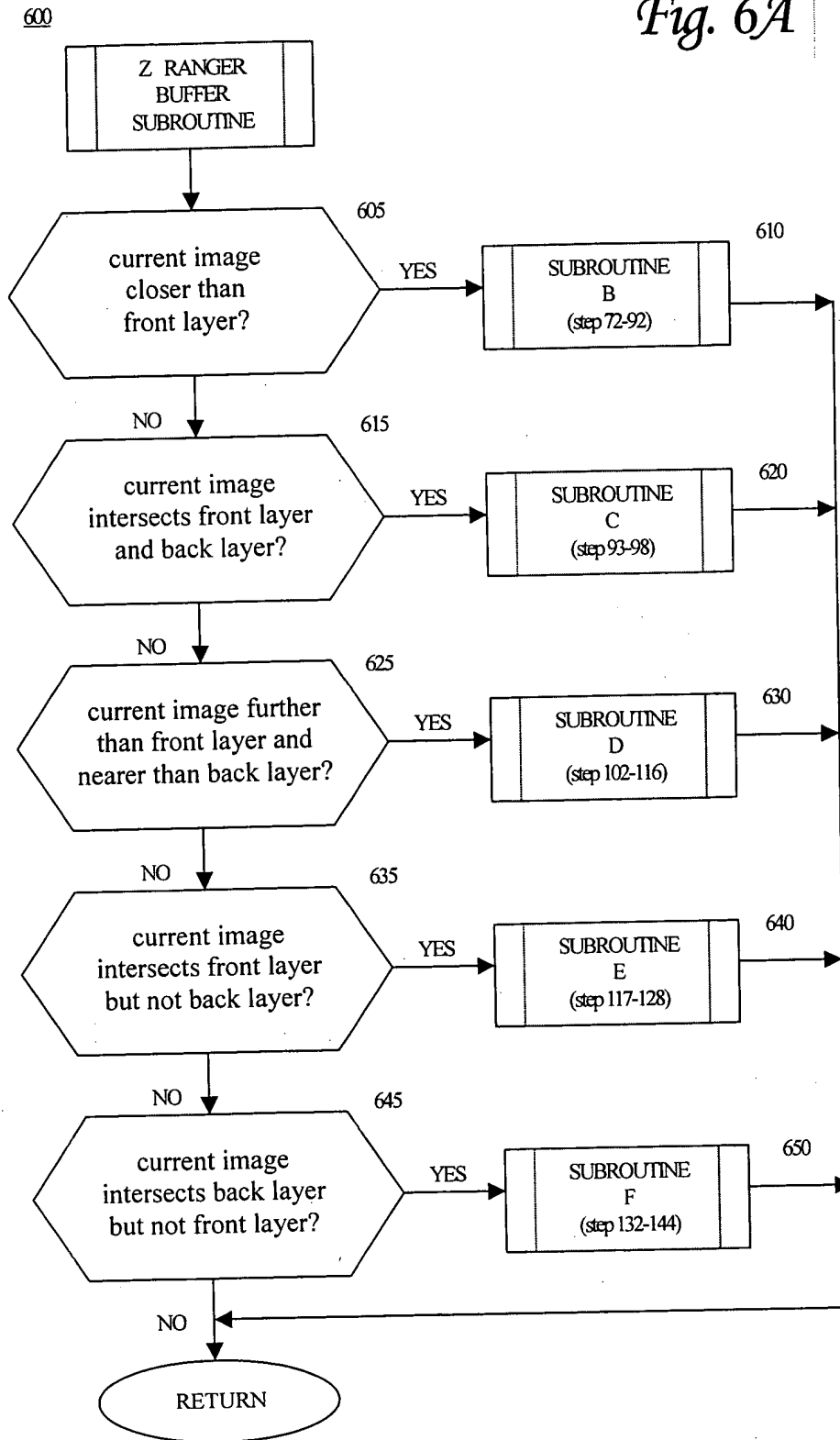


Fig. 6B

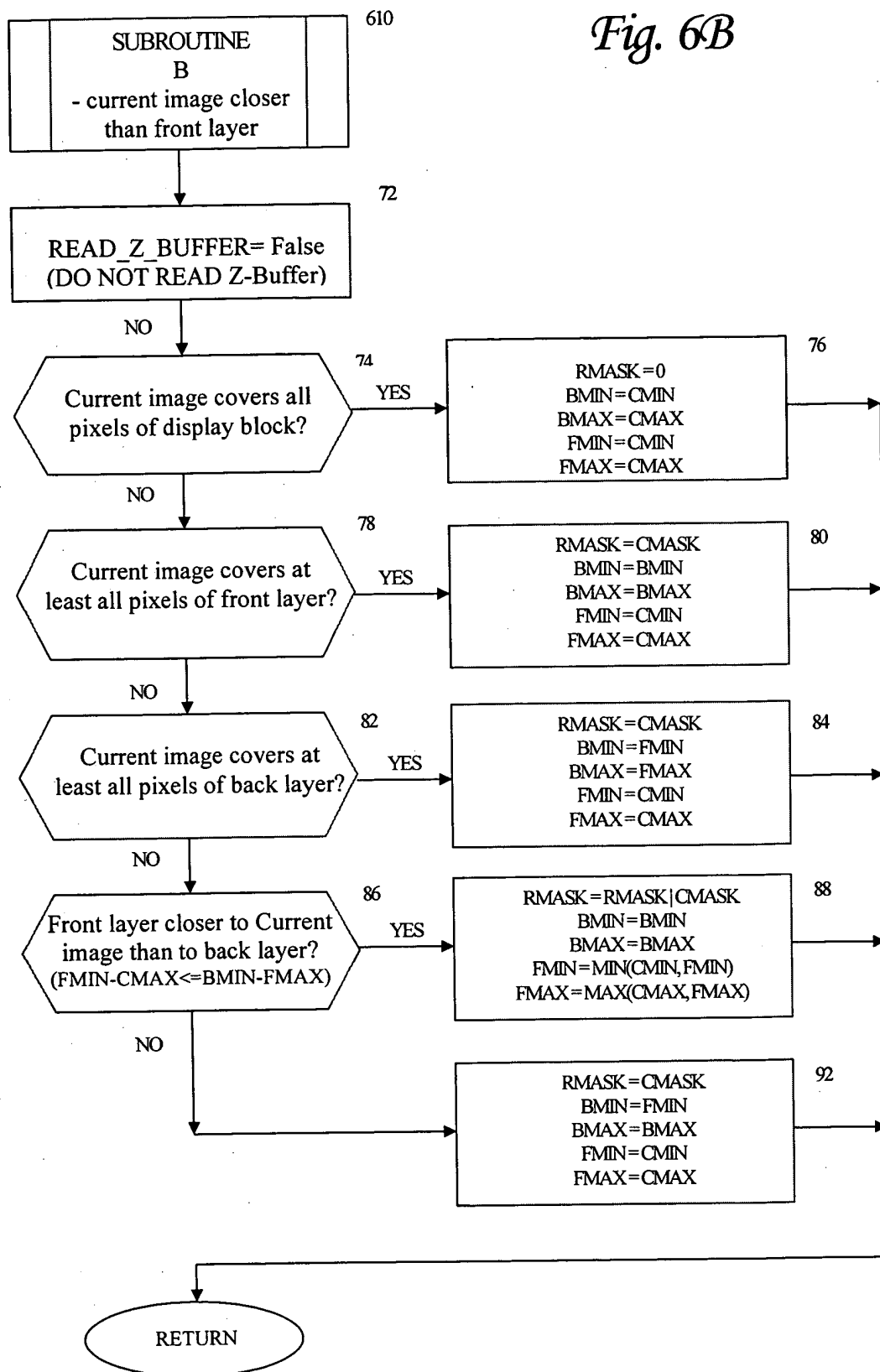
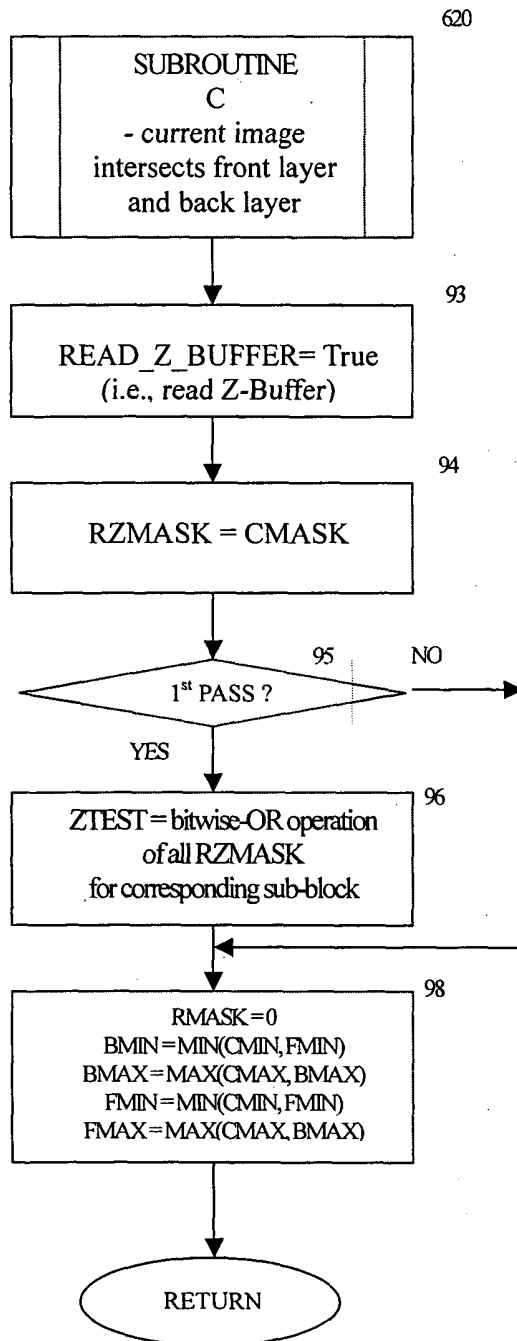


Fig. 6C



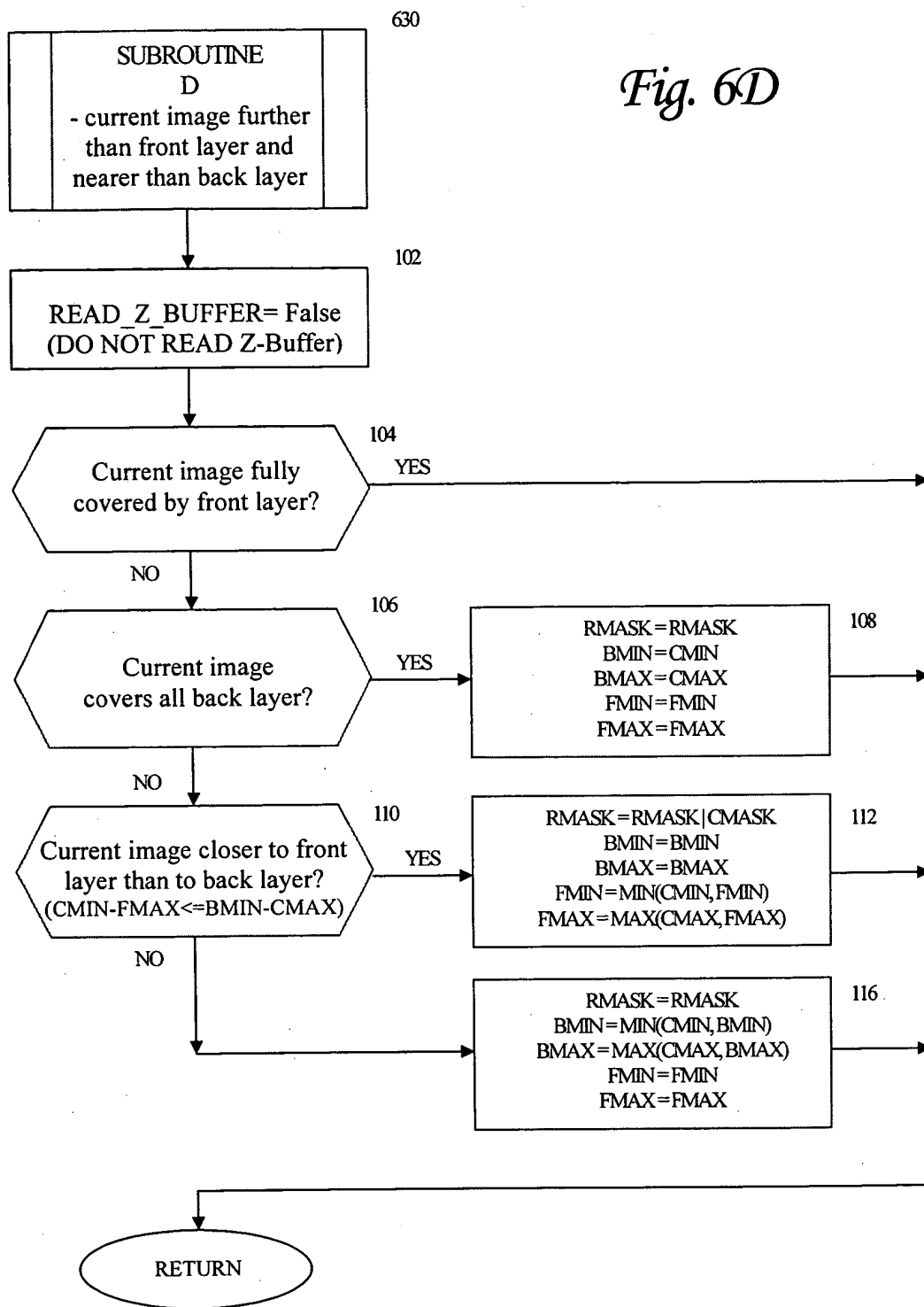
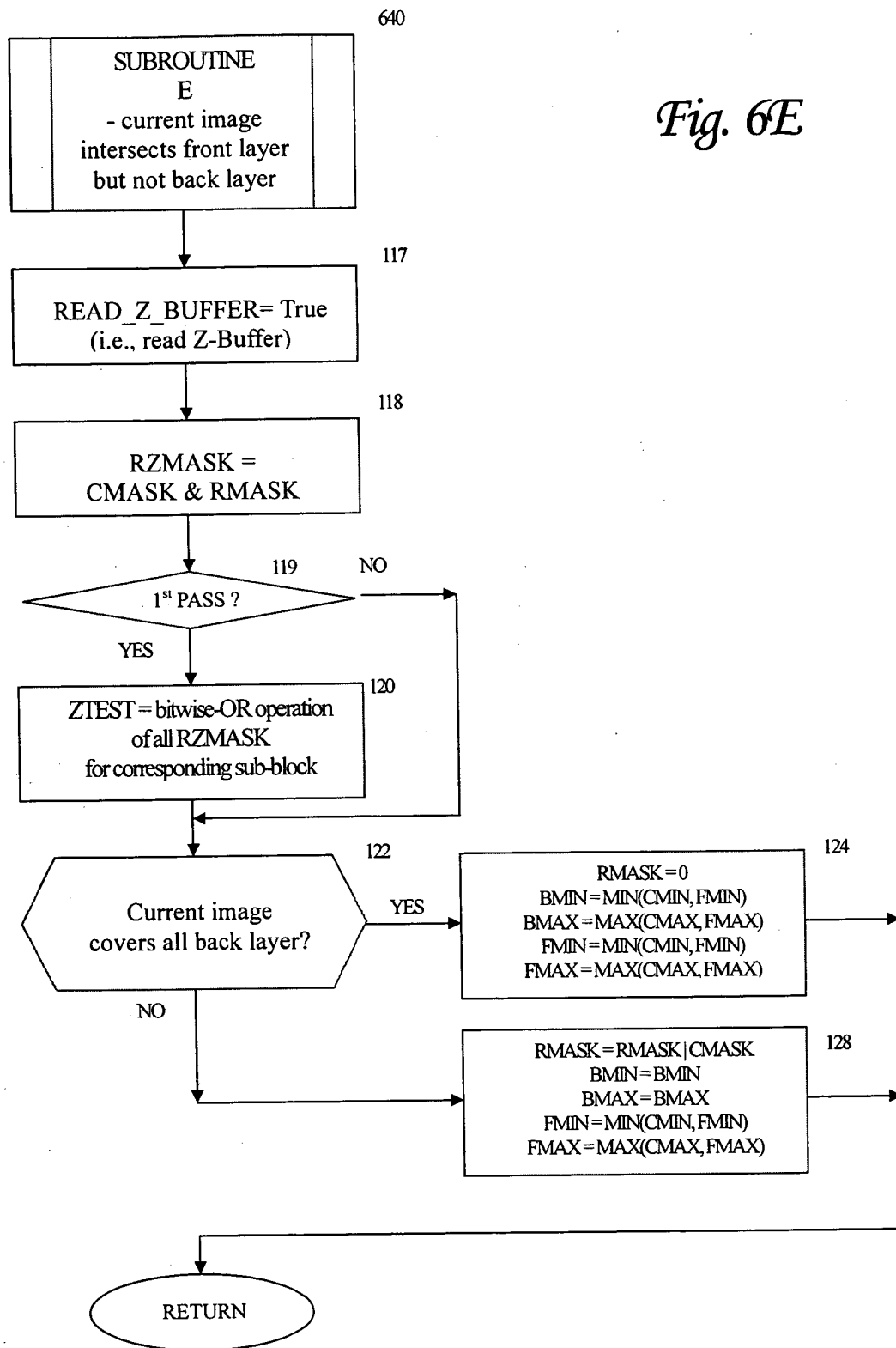


Fig. 6E



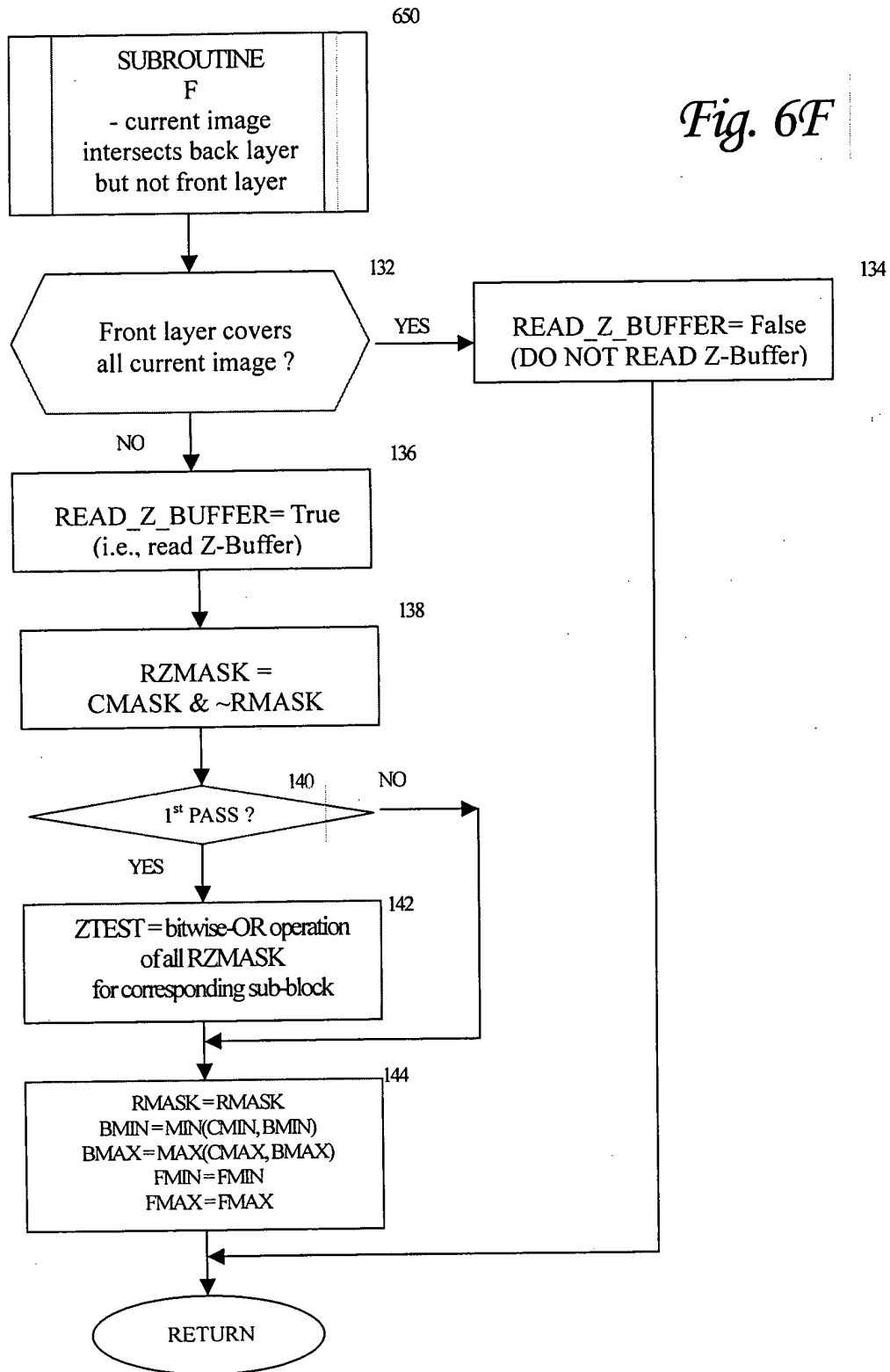
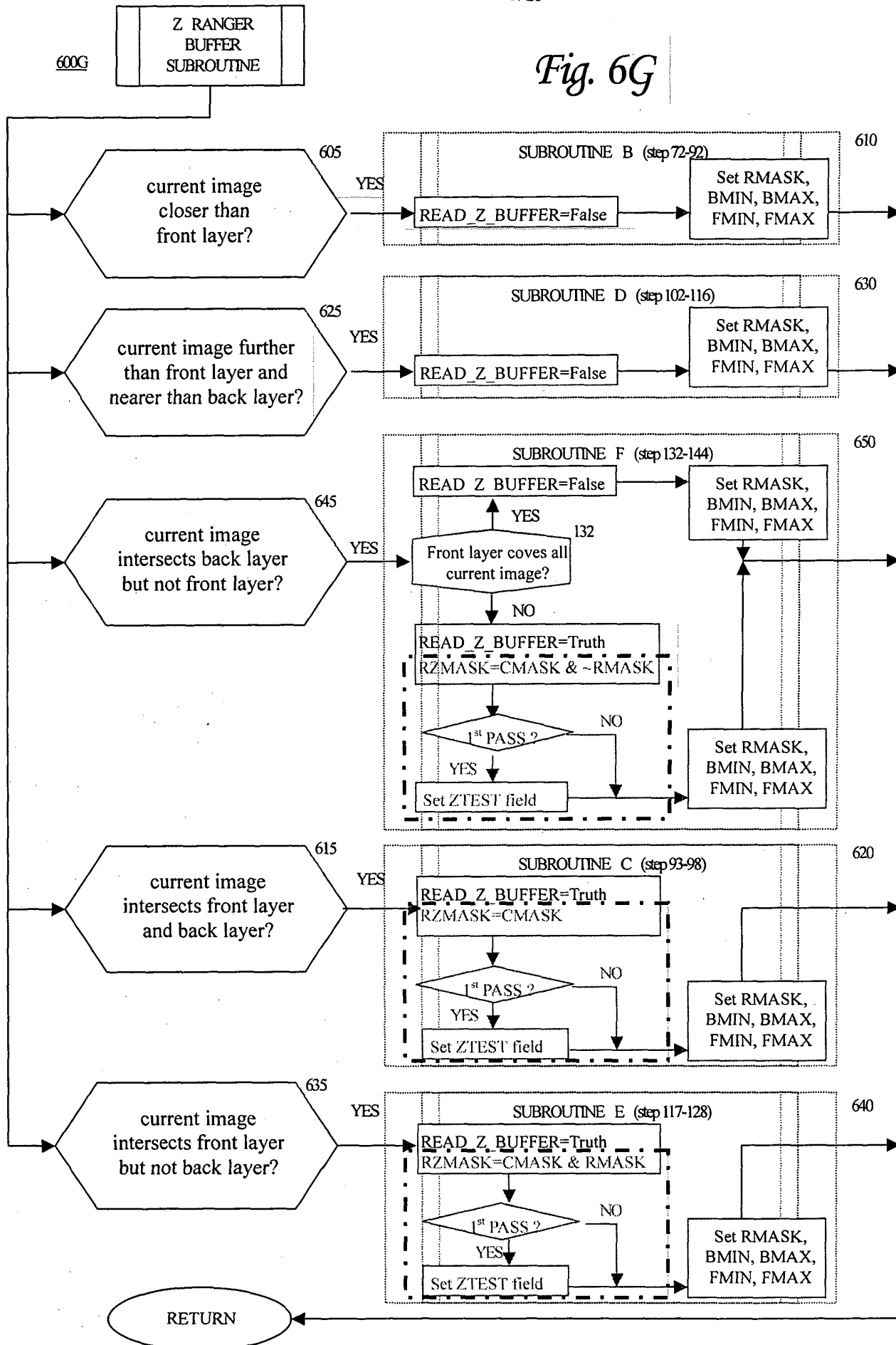


Fig. 6G



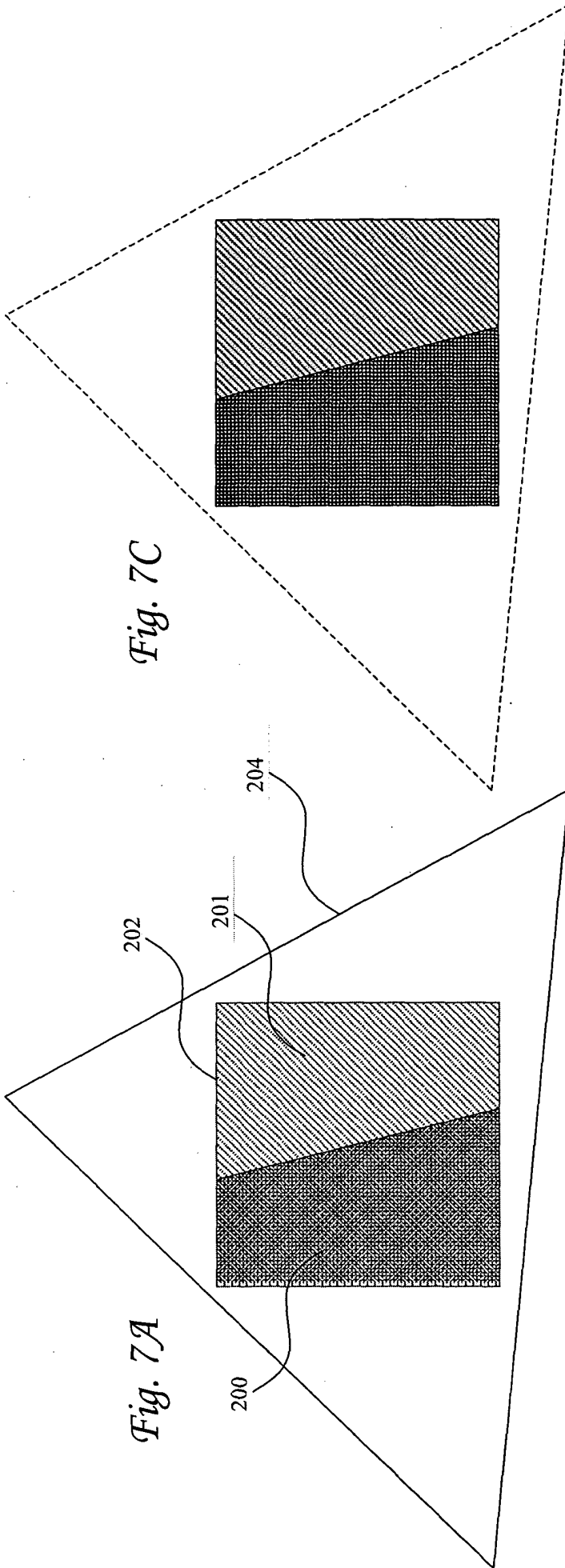


Fig. 7D

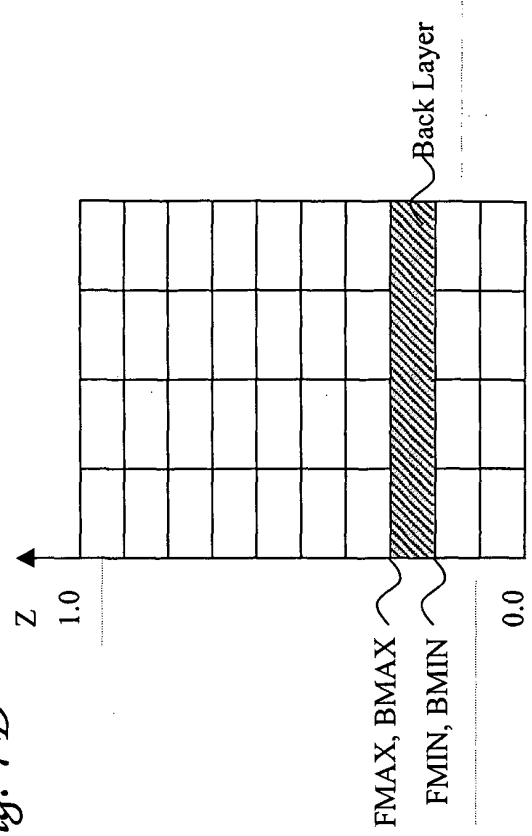
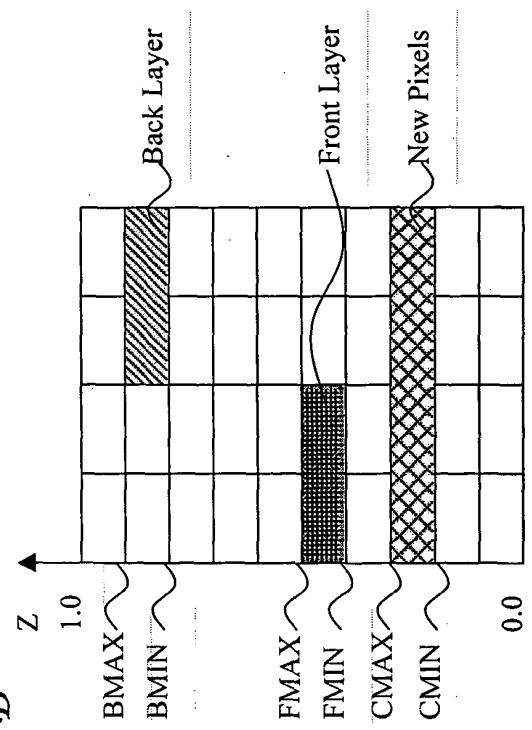
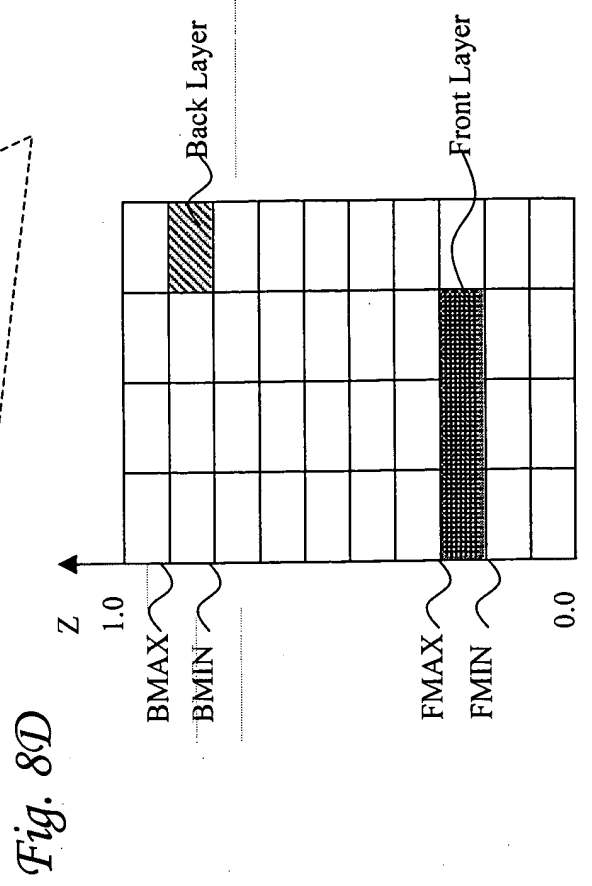
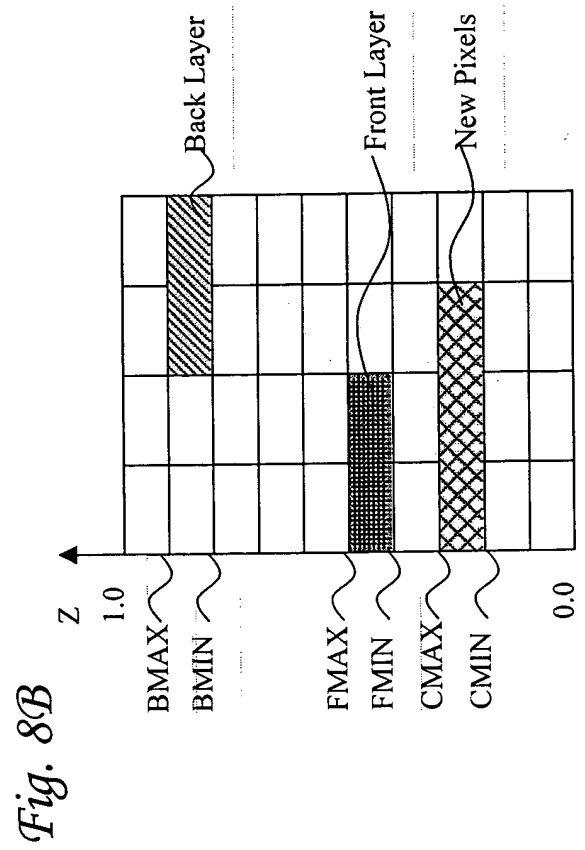
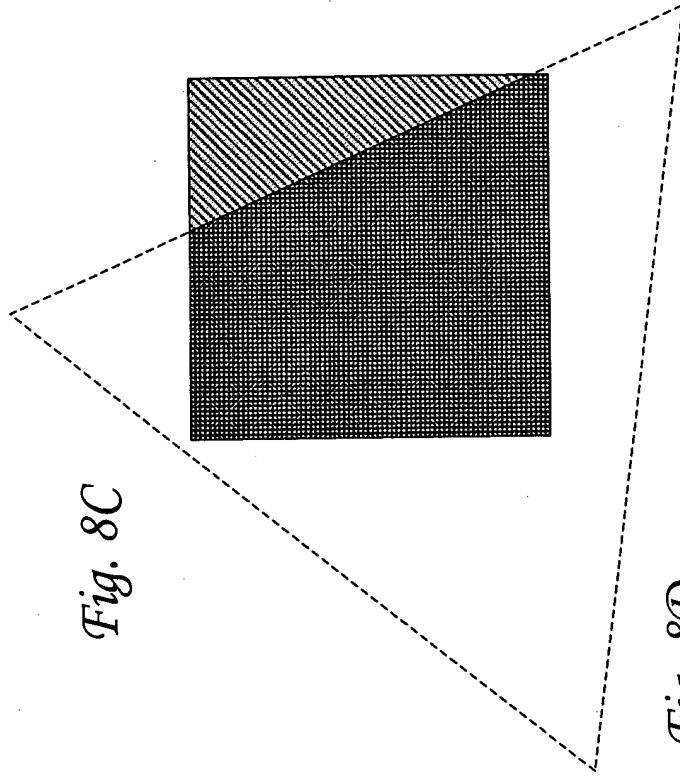
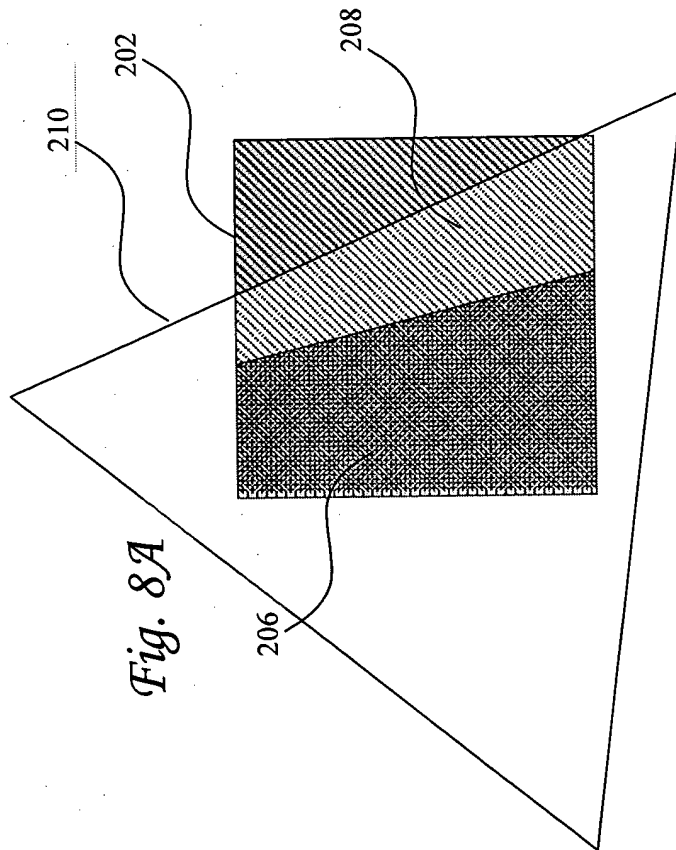


Fig. 7B





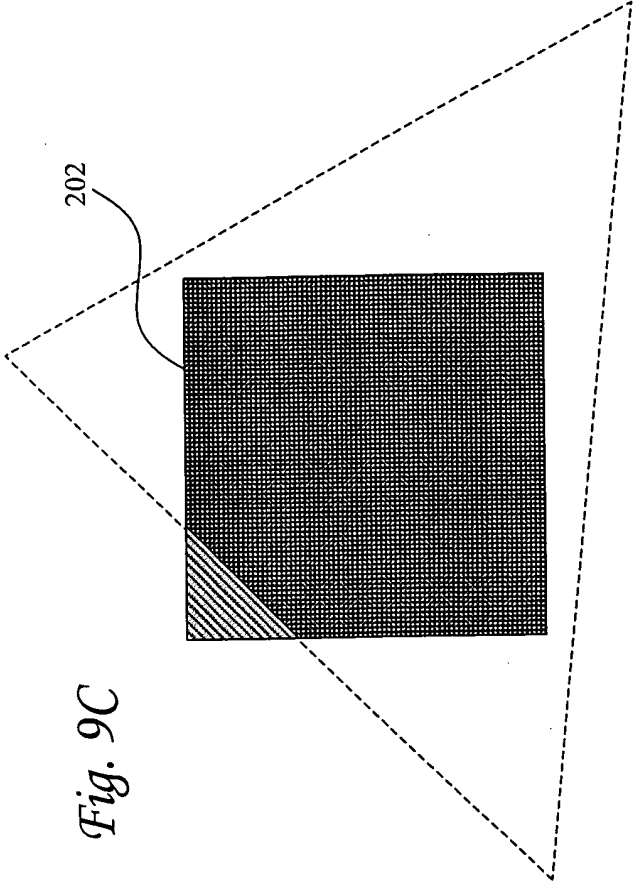
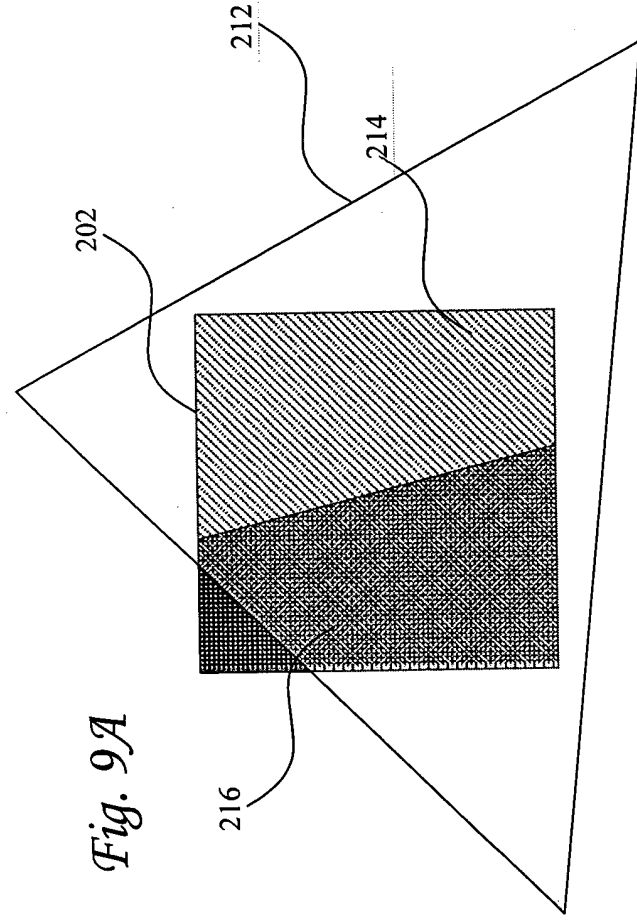


Fig. 9B

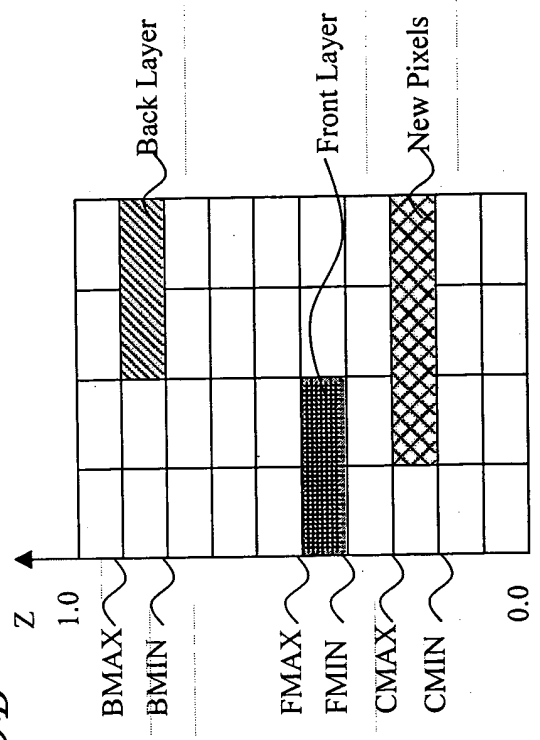


Fig. 9D

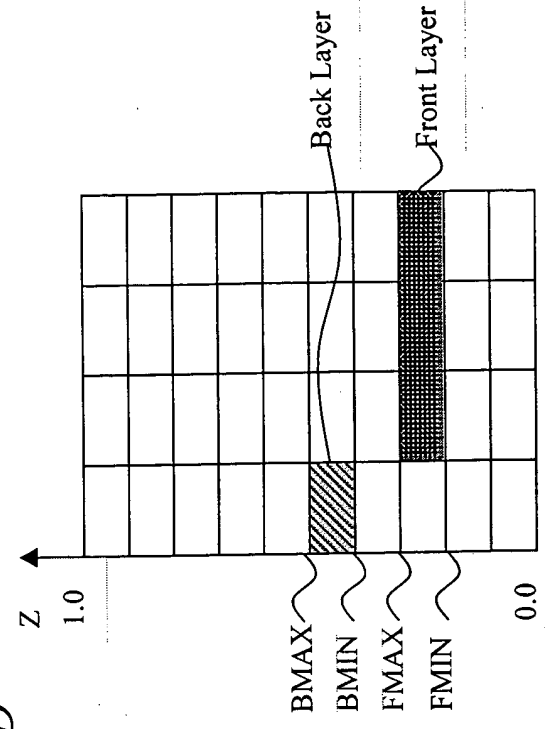


Fig. 10A

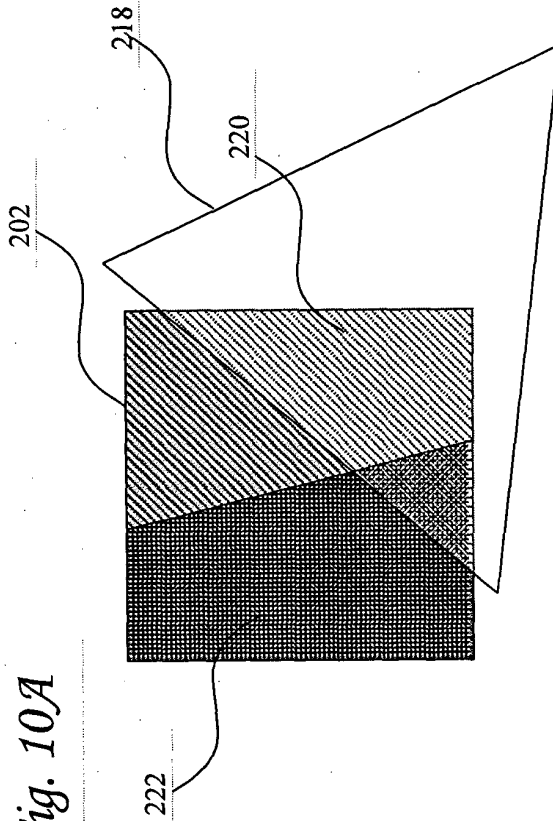


Fig. 10C

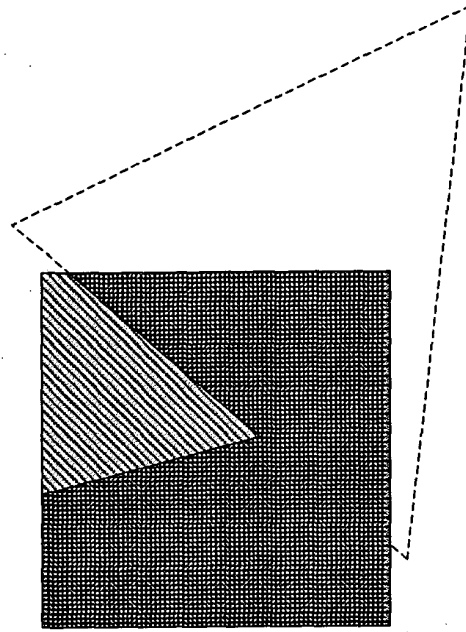


Fig. 10B

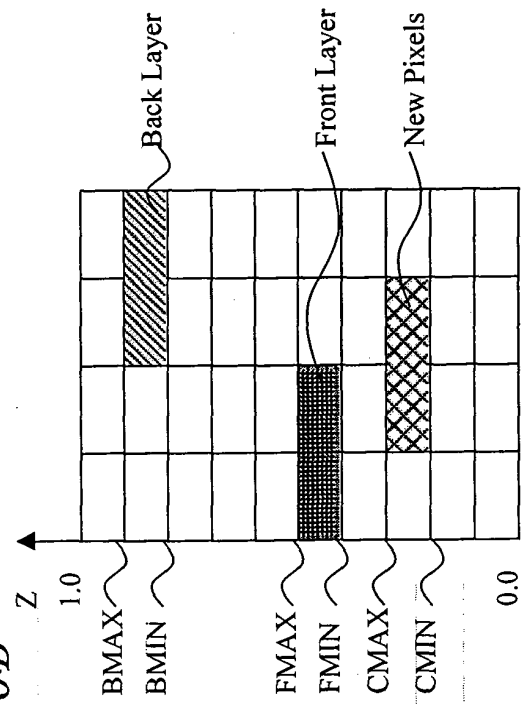


Fig. 10D

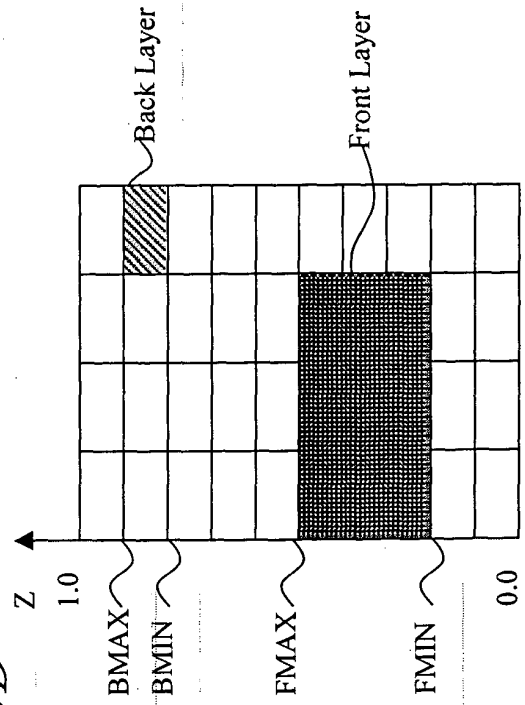


Fig. 10E

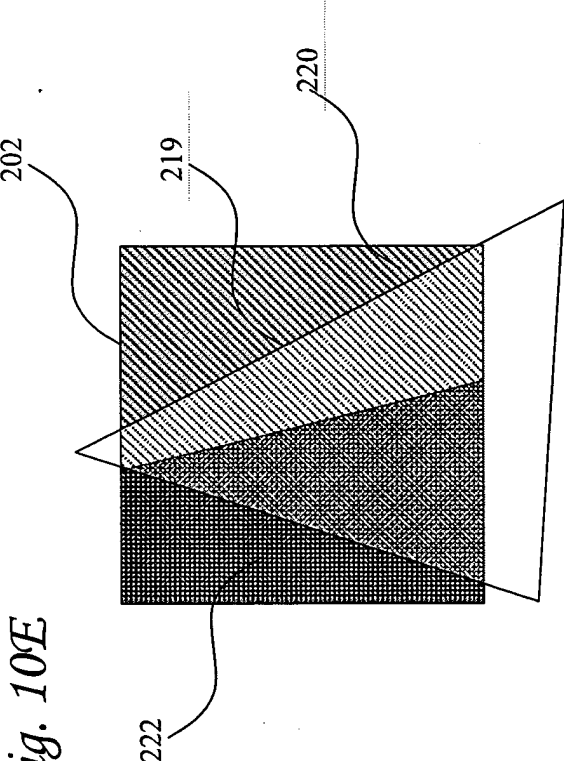


Fig. 10G

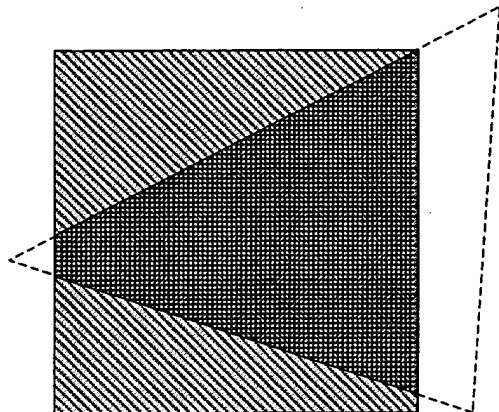


Fig. 10F

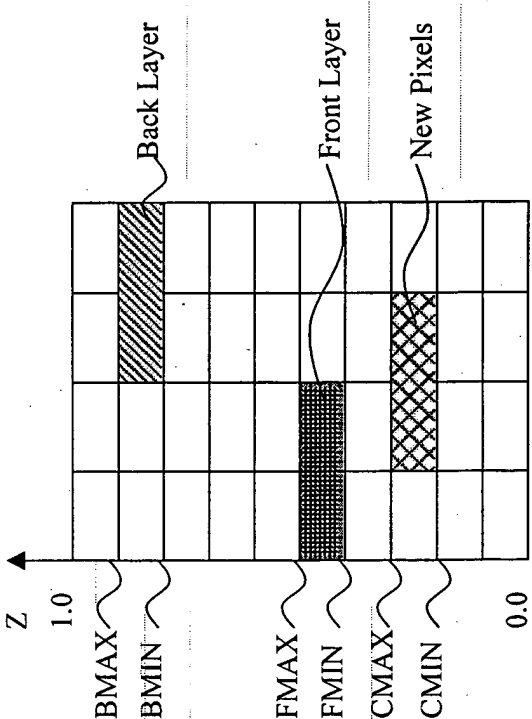
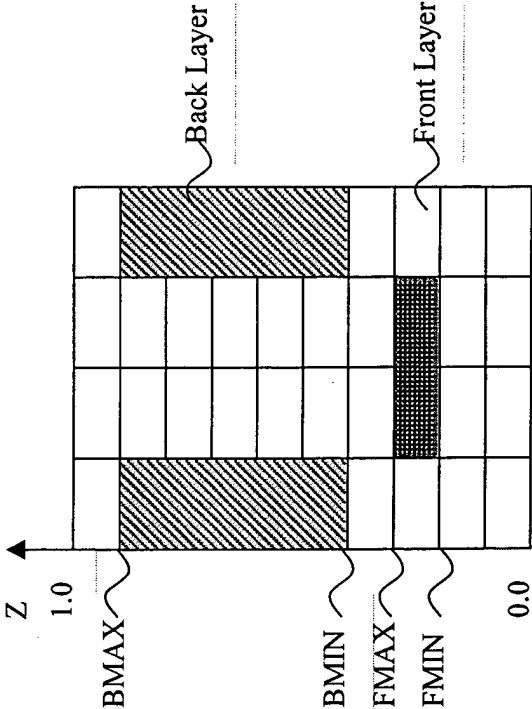


Fig. 10H



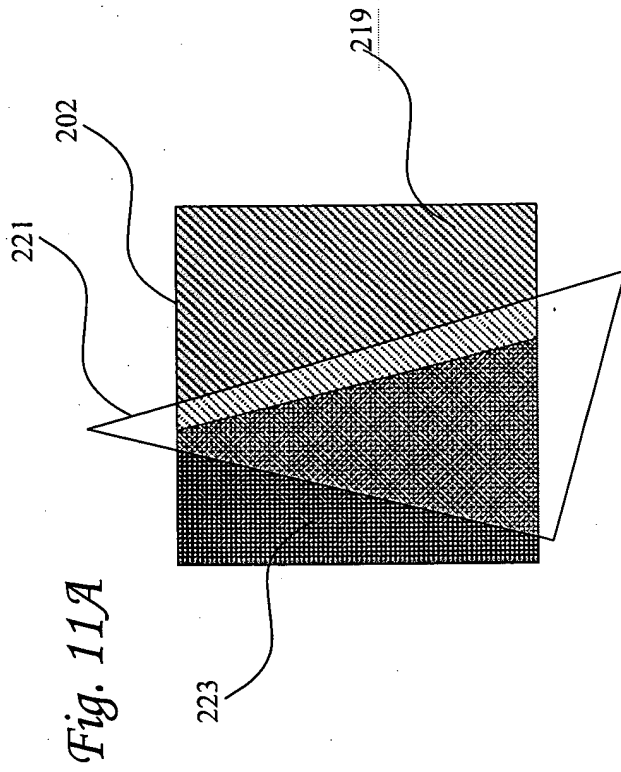


Fig. 11C

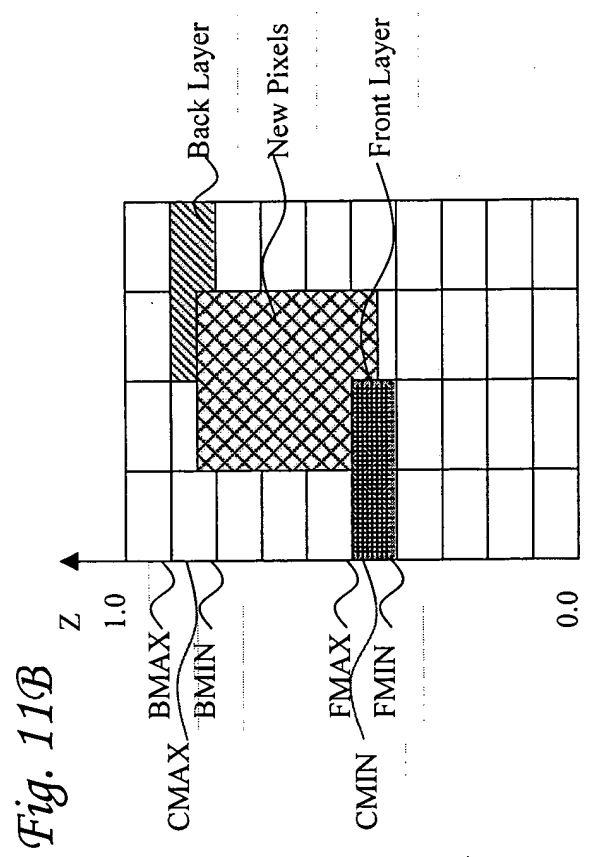
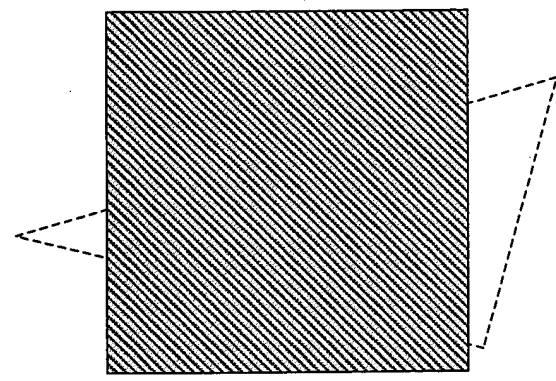
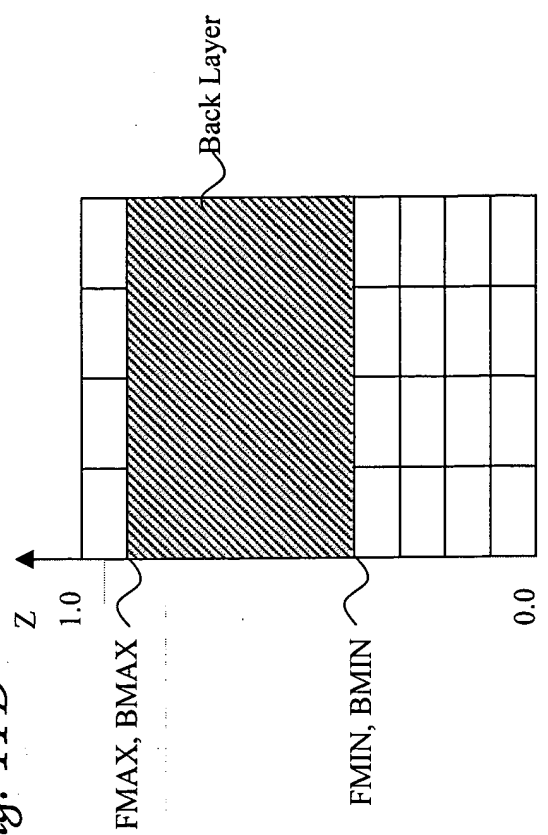


Fig. 11D



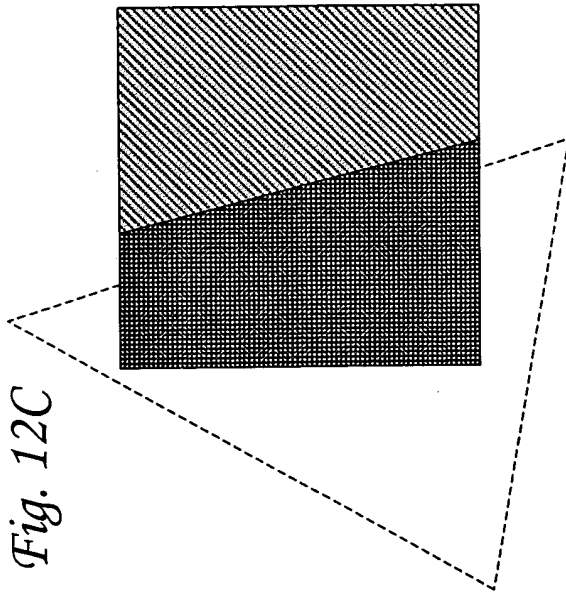


Fig. 12A

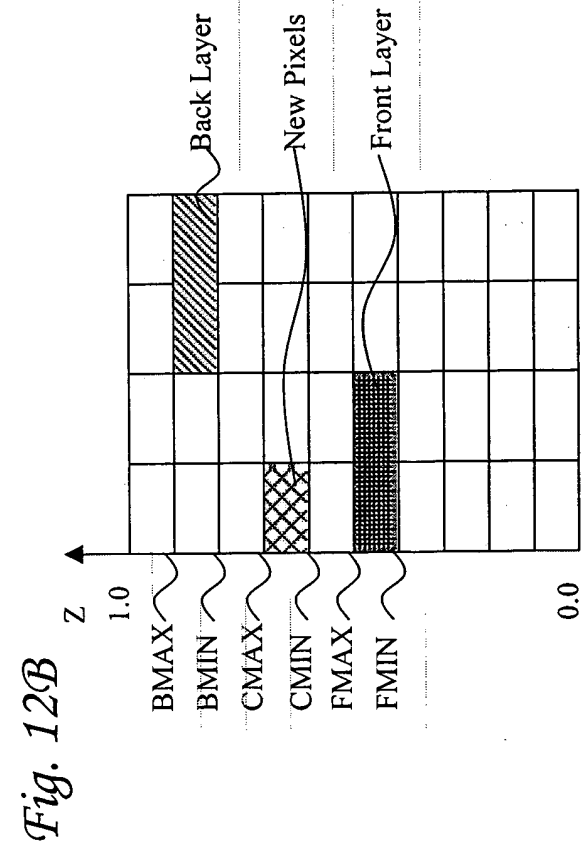


Fig. 12B

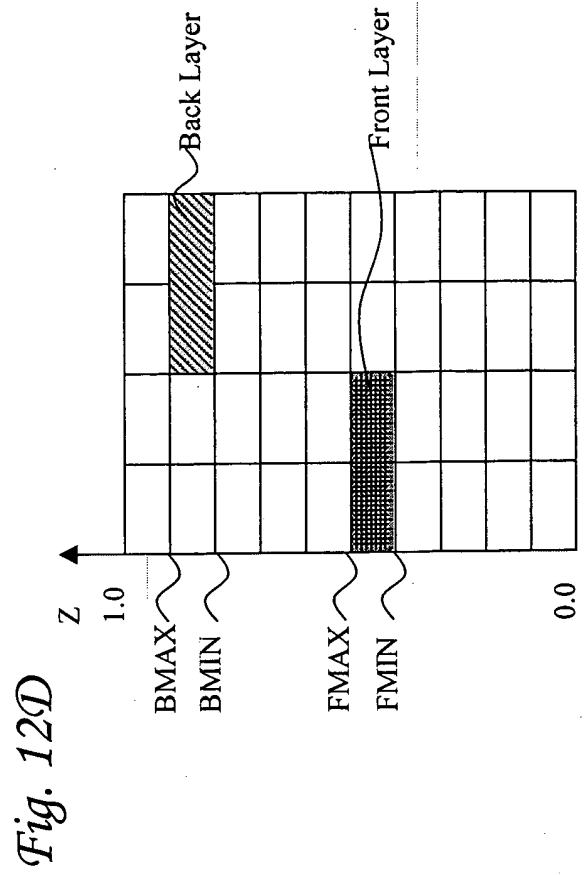


Fig. 12C

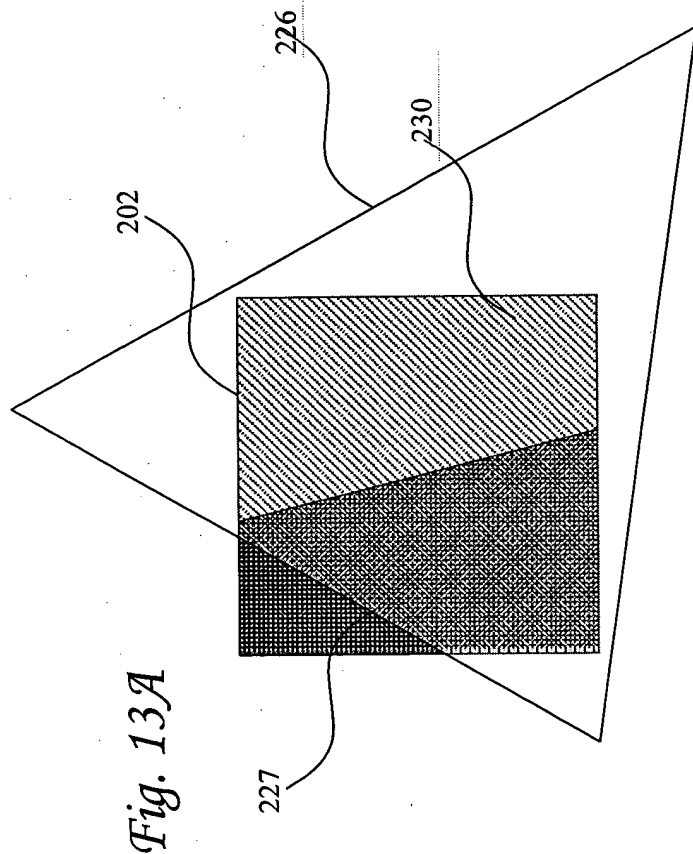


Fig. 13A

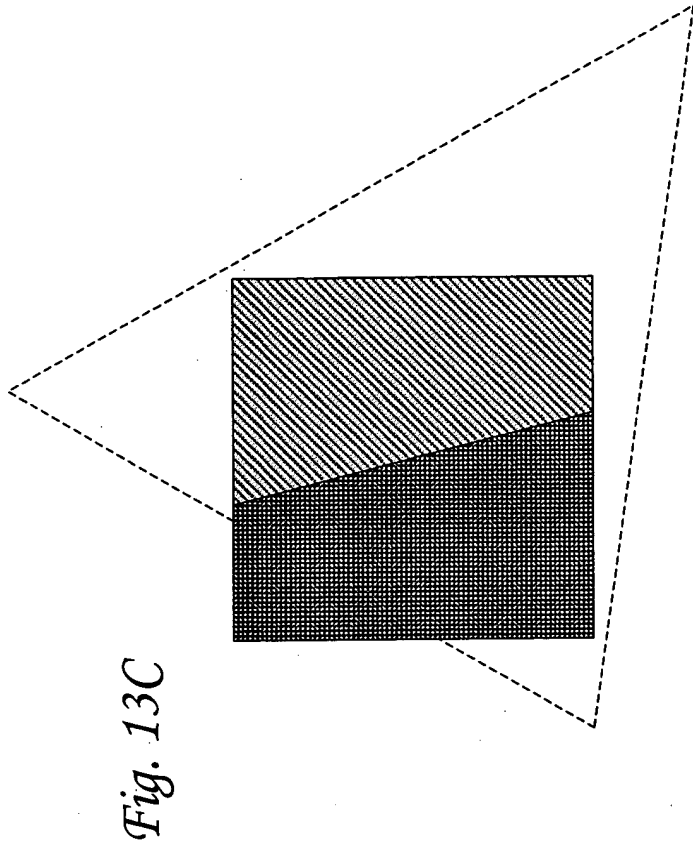


Fig. 13C

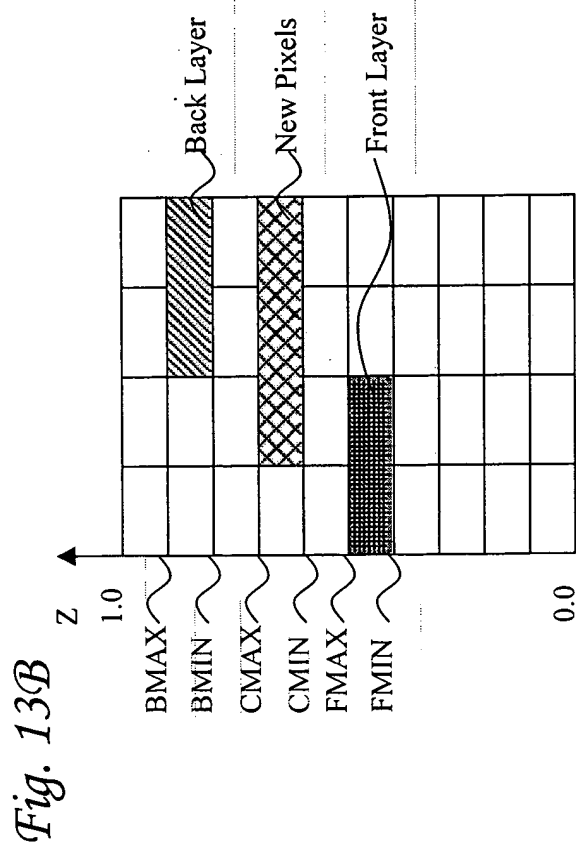


Fig. 13B

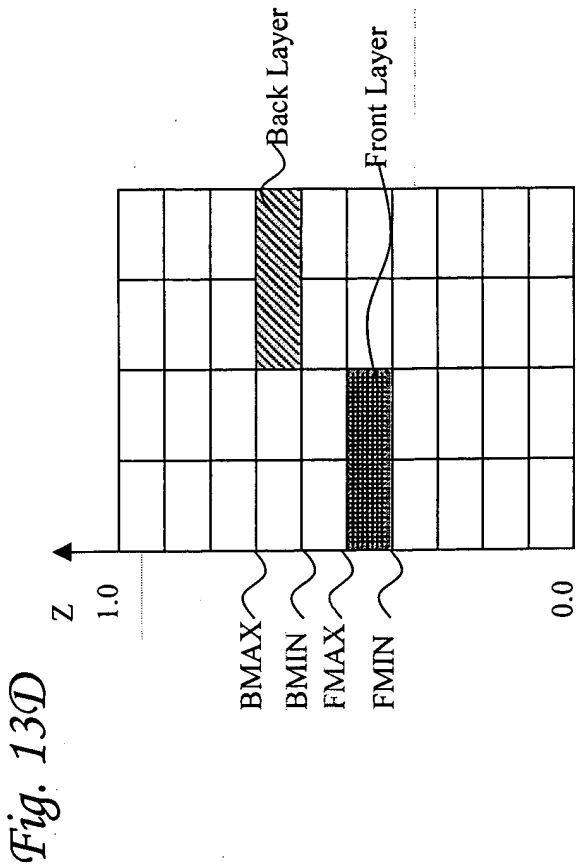


Fig. 13D

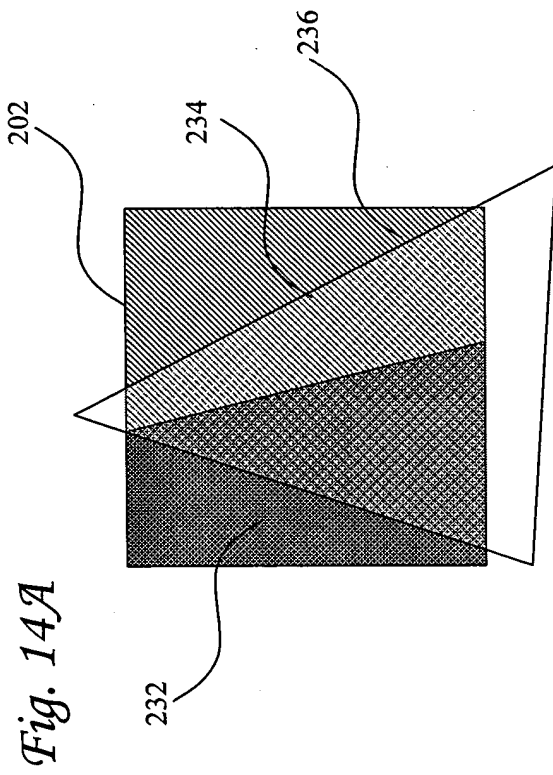


Fig. 14C

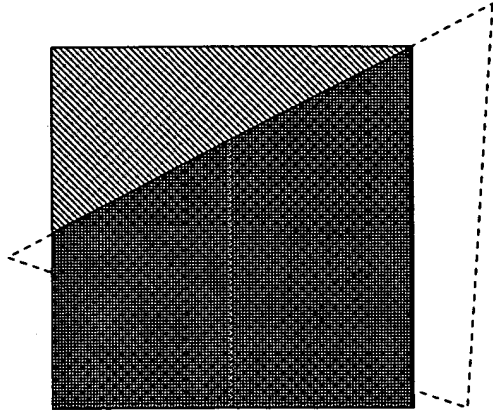


Fig. 14B

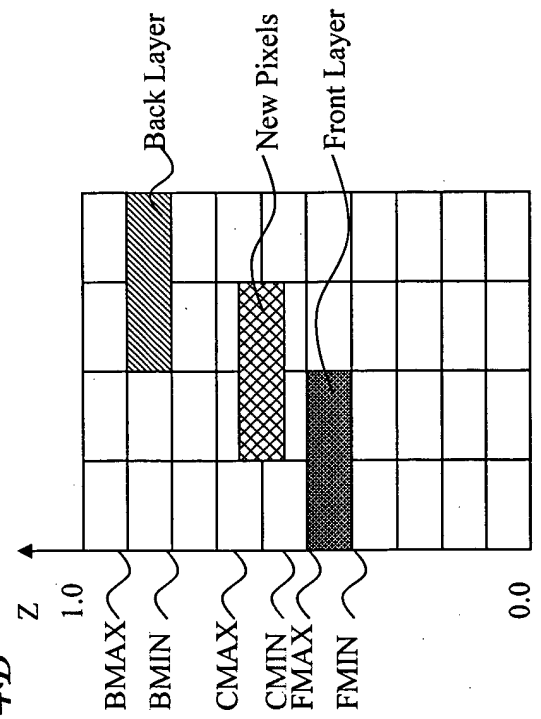


Fig. 14D

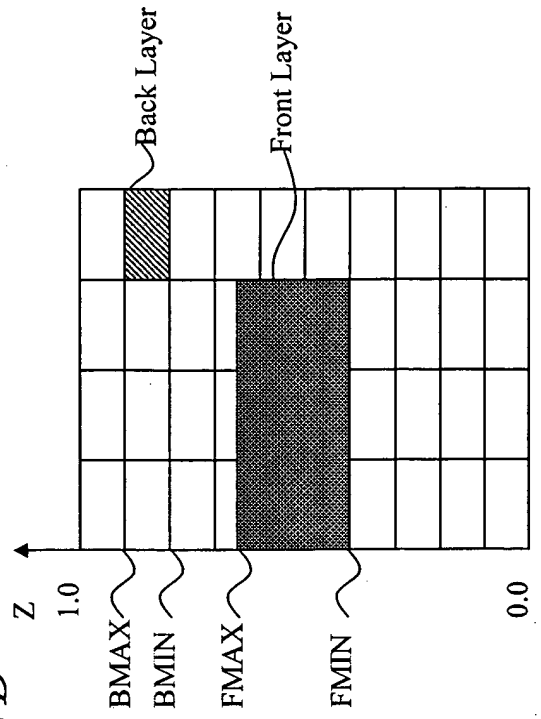


Fig. 14E

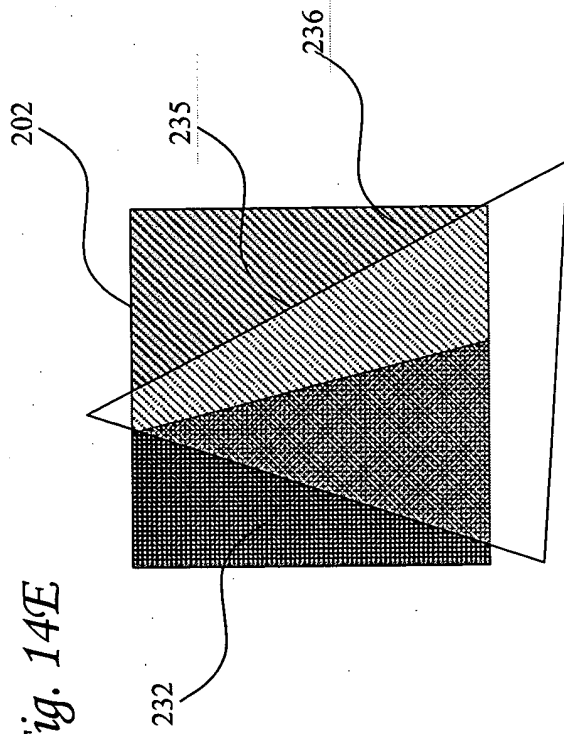


Fig. 14G

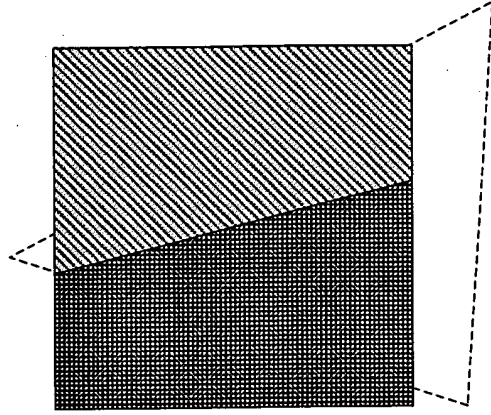


Fig. 14F

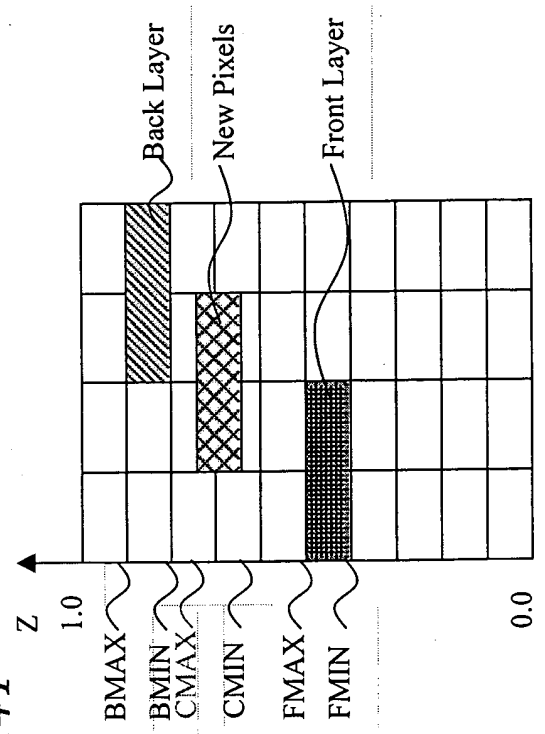
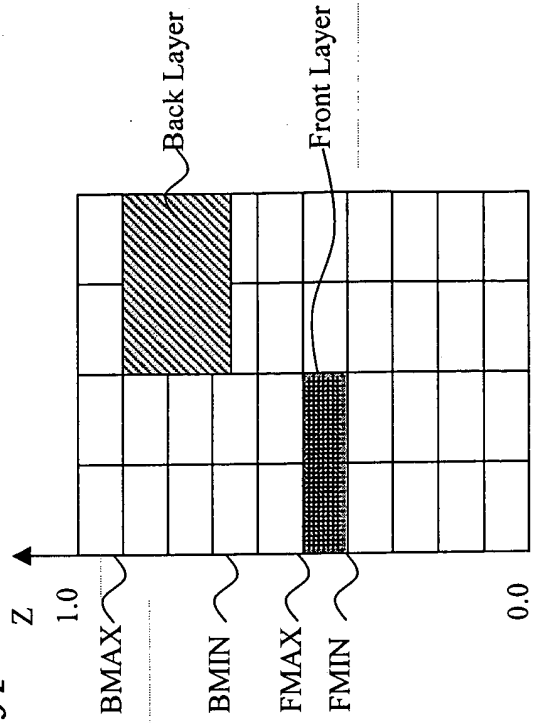


Fig. 14H



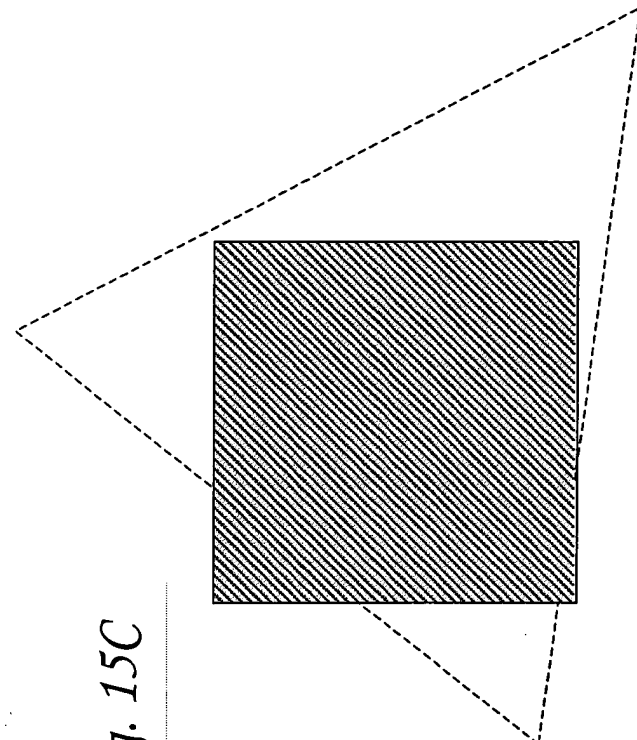


Fig. 15A

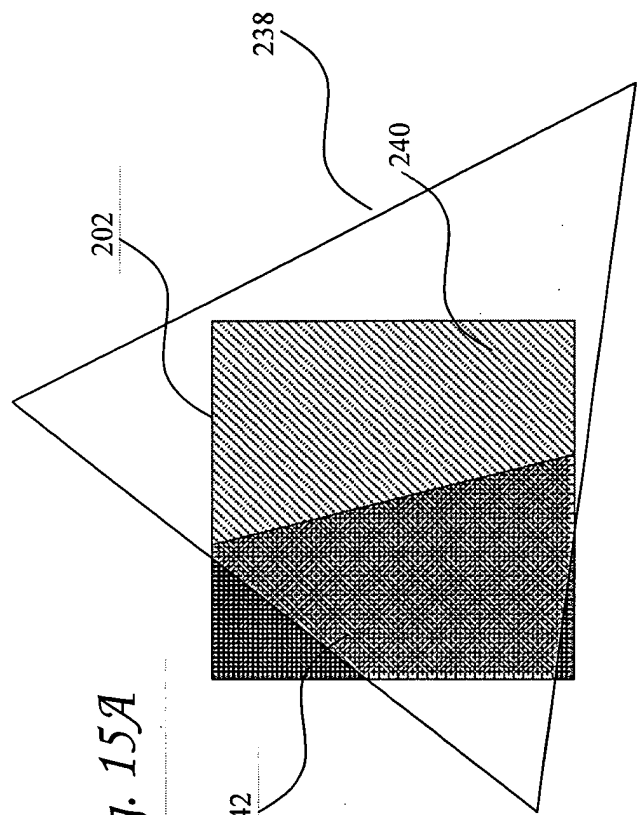


Fig. 15B

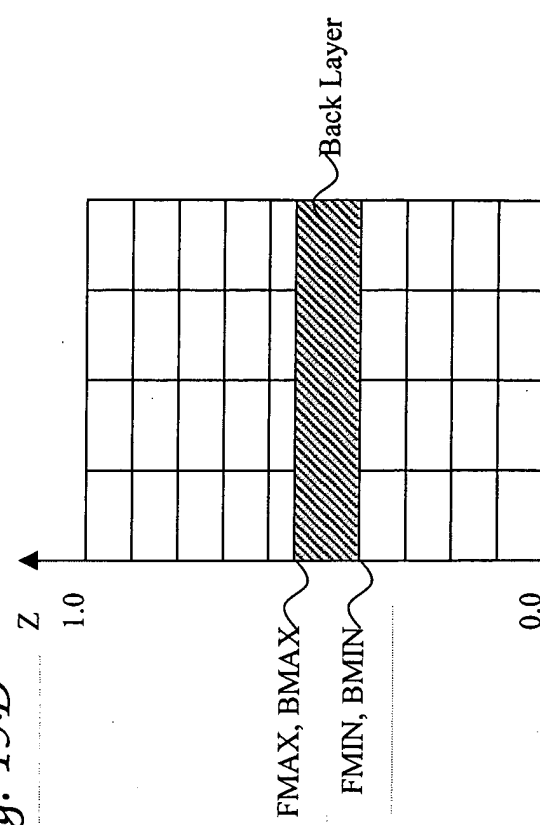


Fig. 15C

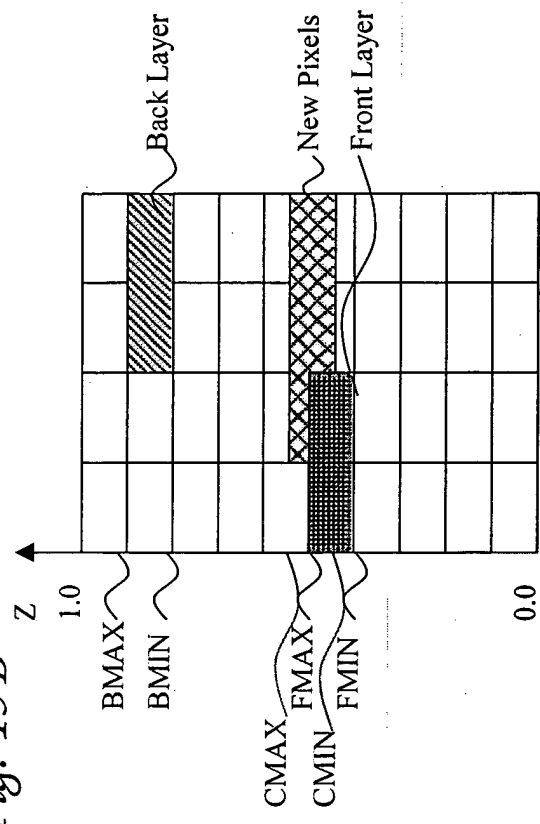


Fig. 15D

Fig. 15E

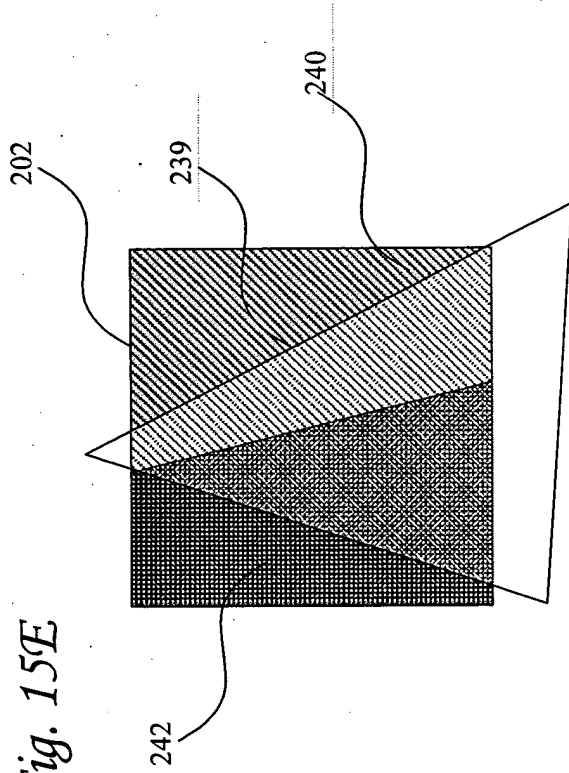


Fig. 15G

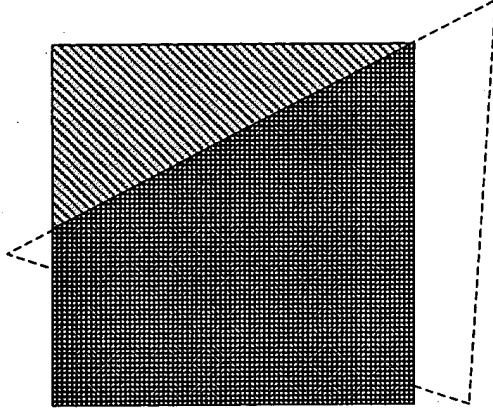


Fig. 15F

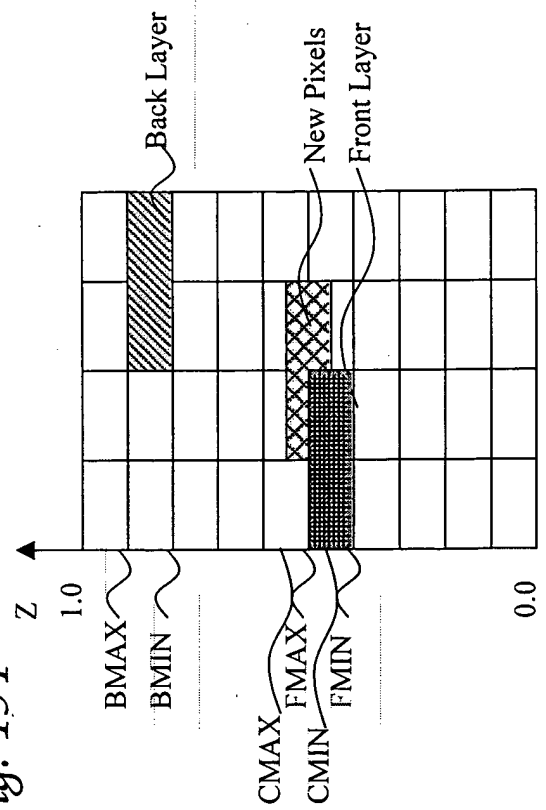
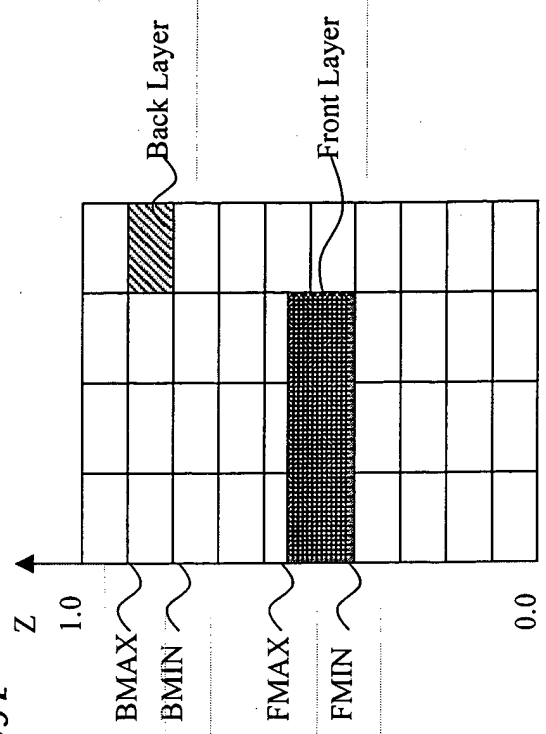


Fig. 15H



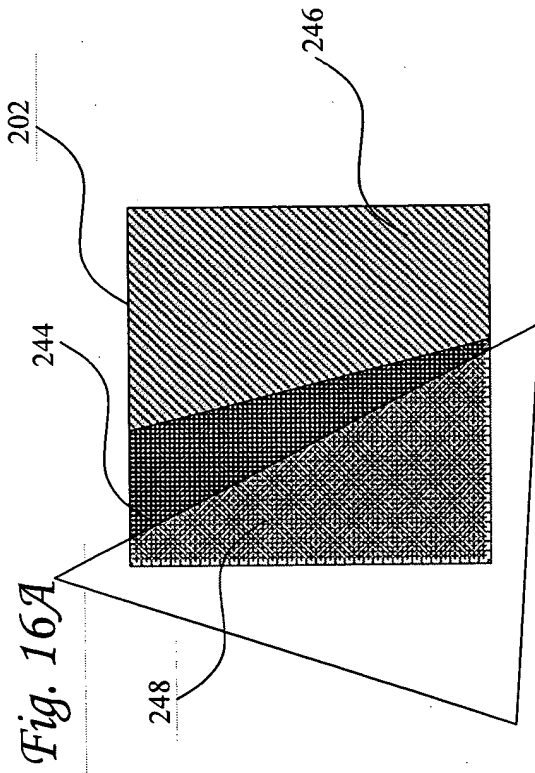


Fig. 16C

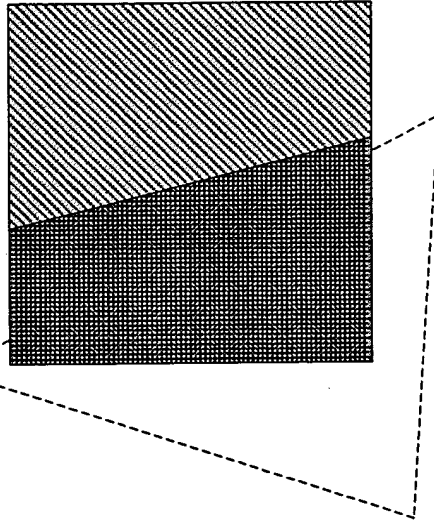


Fig. 16B

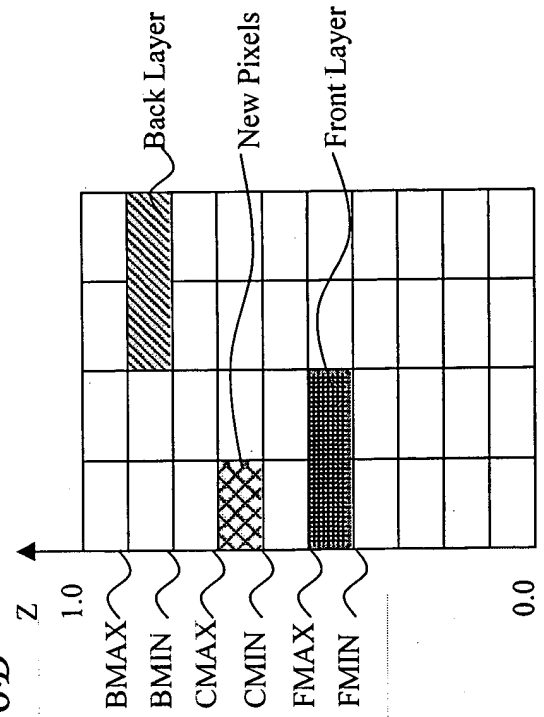


Fig. 16D

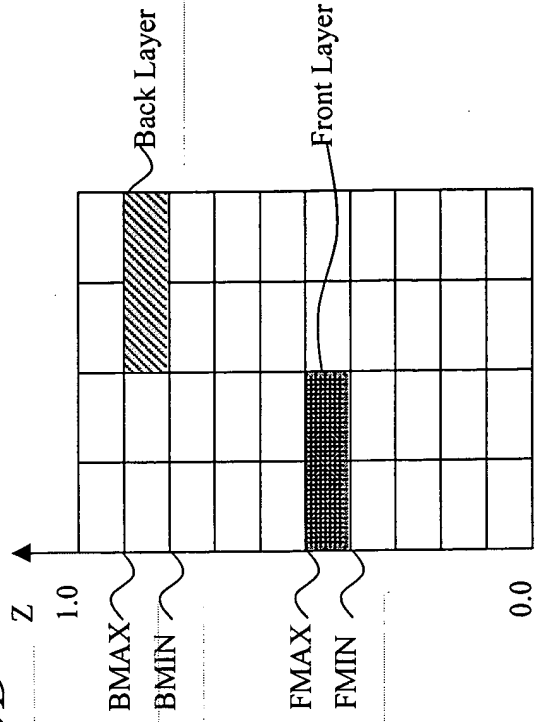


Fig. 16E

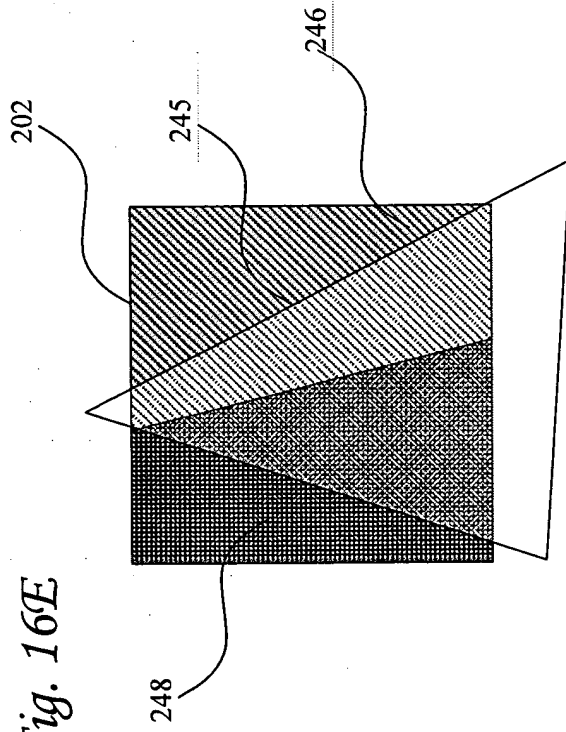


Fig. 16G

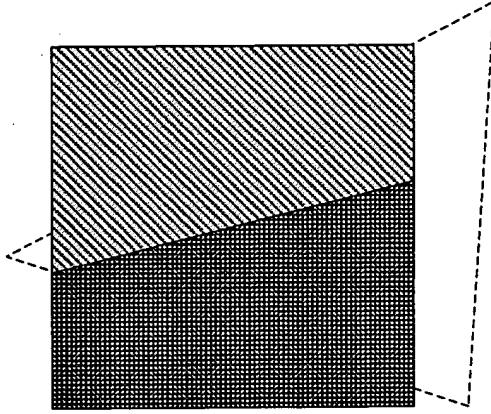


Fig. 16F

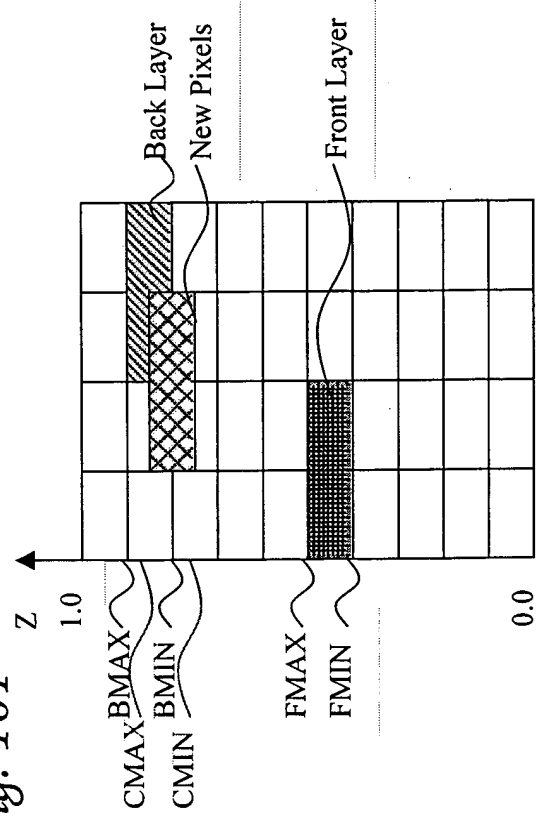


Fig. 16H

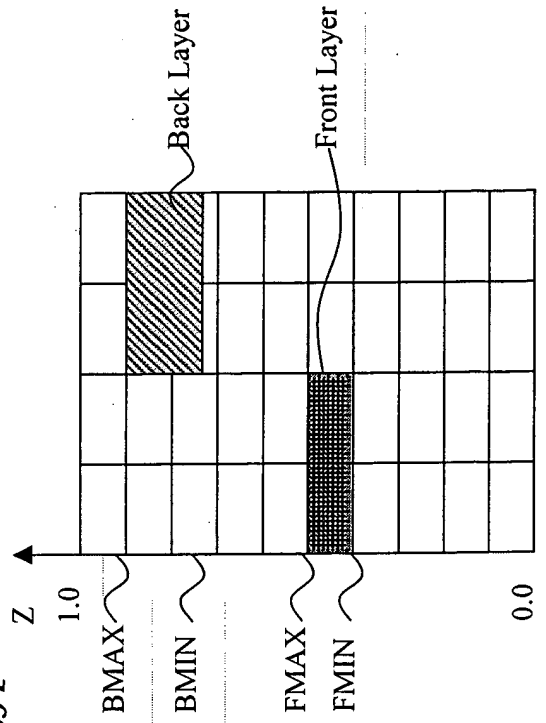


Fig. 17A

RMASK for an 8x8 display block 202

SUB-BLOCK 0 →
SUB-BLOCK 1 →
SUB-BLOCK 2 →
SUB-BLOCK 3 →

1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0

Fig. 17B

CMASK for a current triangle 221

0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Fig. 17C

RZMASK = CMASK

Correspond to SUB-BLOCK 0 → ZTEST[0]=[1]

Correspond to SUB-BLOCK 1 → ZTEST[1]=[1]

Correspond to SUB-BLOCK 2 → ZTEST[2]=[1]

Correspond to SUB-BLOCK 3 → ZTEST[3]=[0]

0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	1	1	1	1	1	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

=> ZTEST[0..3]=[1110]

Fig. 18A

RMASK for an 8x8 display block 202

SUB-BLOCK 0 →
SUB-BLOCK 1 →
SUB-BLOCK 2 →
SUB-BLOCK 3 →

1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0

Fig. 18B

CMASK for a current triangle 238

0	0	0	1	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1
0	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1

Fig. 18C

RZMASK = CMASK & RMASK

Correspond to SUB-BLOCK 0 → ZTEST[0]=[0]

Correspond to SUB-BLOCK 1 → ZTEST[1]=[1]

Correspond to SUB-BLOCK 2 → ZTEST[2]=[1]

Correspond to SUB-BLOCK 3 → ZTEST[3]=[1]

0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0

=> ZTEST[0..3]=[0111]

Fig. 19A

RMASK for an 8x8 display block 202

SUB-BLOCK 0 →
SUB-BLOCK 1 →
SUB-BLOCK 2 →
SUB-BLOCK 3 →

1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0

Fig. 19B

CMASK for a current triangle 250

0	0	0	1	0	0	0	0
0	0	1	1	1	0	0	0
0	0	1	1	1	0	0	0
0	0	1	1	1	1	0	0
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1

Fig. 19C

RZMASK = CMASK & ~RMASK

Correspond to SUB-BLOCK 0 → ZTEST[0]=[1]

Correspond to SUB-BLOCK 1 → ZTEST[1]=[1]

Correspond to SUB-BLOCK 2 → ZTEST[2]=[1]

Correspond to SUB-BLOCK 3 → ZTEST[3]=[1]

0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0
0	0	0	0	1	1	0	0
0	0	0	0	0	1	1	0
0	0	0	0	0	1	1	0
0	0	0	0	0	1	1	0
0	0	0	0	0	1	1	1

⇒ ZTEST[0..3]=[1111]

Fig. 20A

RMASK for an 8x8 display block 202

1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0
SB0'	SB1'	SB2'	SB3'				

Fig. 20B

CMASK for a current triangle 250

0	0	0	1	0	0	0	0
0	0	1	1	1	0	0	0
0	0	1	1	1	0	0	0
0	0	1	1	1	1	0	0
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1

Fig. 20C

RZMASK = CMASK & ~RMASK

Correspond to SUB-BLOCK 0' → ZTEST[0]=[0]

Correspond to SUB-BLOCK 1' → ZTEST[1]=[1]

Correspond to SUB-BLOCK 2' → ZTEST[2]=[1]

Correspond to SUB-BLOCK 3' → ZTEST[3]=[1]

0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0
0	0	0	0	1	1	0	0
0	0	0	0	1	1	0	0
0	0	0	0	0	1	1	0
0	0	0	0	0	1	1	0
0	0	0	0	0	1	1	1
SB0'	SB1'	SB2'	SB3'				

=> ZTEST[0..3]=[0111]